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FINAL DESIGN REPORT

FOR

ADVANCED MEMORY AND MEMORY SEQUENCER
(MAMS)

6 MARCH 1970

CONTRACT NO. NAS5-21035

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PREPARED BY

RADIATION INCORPORATED

(SUBSIDIARY OF HARRIS-INTERTYPE CORPORATION)

PO BOX 37

MELBOURNE, FLA

FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND



RADIATION
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GODDARD SPACE FLIGHT CENTER

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LIST OF ACRONYMS

DTL	Diode-Transistor Logic
LSB	Least Significant Bit
LSI	Large Scale Integration
MAMS	Memory and Memory Sequencer
MOS	Metallic Oxide Semiconductor
MSB	Most Significant Bit
MSI	Medium Scale Integration
RAM	Random Access Memory
ROM	Read-Only Memory
VIP	Versatile Information Processor

1.0 INTRODUCTION

The object of this report is to describe the results of the work performed under study contract NAS5-21035, advanced Memory and Memory Sequencer (MAMS). This study was undertaken to investigate the feasibility of reducing the physical size of the Nimbus-D VIP memory and memory sequencer modules through the use of LSI techniques, while retaining their functional capacity. The report describes the design goals, priorities, and functional characteristics, and gives a detailed view of the electrical and mechanical design approaches employed. It concludes that a system using MOS technology for both memories and logic, dissipating slightly over 1 watt, can be packaged in a Nimbus size 1/0 housing without undue design risk. The approach makes maximum use of microprogramming and, except for some custom control logic, uses standard parts and techniques. It is recommended that a system such as described herein, be developed for use with Nimbus and other information-gathering projects which place a premium on low size, weight, and power, yet require a large and flexible information processor.

2.0 DESIGN REPORT SUMMARY

2.1 Background

Designers of information handling equipment for on-board spacecraft applications are frequently confronted with conflicting requirements. They are asked to maintain, or even increase, the complexity and capacity of the equipment while sharply reducing size and weight. As space agency officials contemplate more extensive investigations by unmanned scientific satellites, they are asking specific manufacturers to reduce the size and weight of certain packages which they had previously specified at much larger figures. Thanks to the advent of MSI and LSI monolithic circuits, the industry is finding new ways to meet these requirements without degradation in capacity or operating performance.

As part of the original Nimbus program, the NASA Goddard Space Flight Center in Greenbelt, Md., had awarded a contract to Radiation Incorporated, subsidiary of Harris-Intertype Corporation, for a Versatile Information Processor (VIP) with a random-access memory programmer comprised of three sections with a total size of 12 inches by 6 inches by 6 1/2 inches. The three sections consist of two memory modules and a memory controller, or sequencer. More recently, for advanced versions of Nimbus, NASA Goddard specified a vast reduction in size, and a design feasibility study was initiated aimed at reducing the size of the memory and memory sequencer by a factor of 6. The new MAMS was specified at 2 inches by 6 inches by 6 1/2 inches. The other portions of the VIP system remained the same, both physically and functionally. Because the Advanced MAMS, as the new and smaller memory and memory sequencer is called, was designed for flexible interfacing, it can be applied to a wide range of spacecraft and satellite information processing equipment, with comparable savings in size and weight.

2.2 Functional Description

The memory and memory sequencer performs the basic function of synchronizing and forwarding data between the satellite or spacecraft and a ground station. The memory has no capacity for prolonged storage of collected data. In conjunction with the Nimbus VIP, as well as any other similar information handling and processing system, the memory provides nondestructive read-out (NDRO) of predetermined data sampling formats and in-flight programmable subroutines. The memory sequencer portion provides primary control and output conditioning for the memory. Briefly, the sequencer takes channel addresses from the memory upon command from a formatter module, which executes the operations specified by the selected memory word.

2.3 Design Approach

The study contract did not specify how the size reduction was to be accomplished; it merely specified that operational specifications must be maintained. Various component and circuit tradeoffs had to be made — such as whether to use MOS or bipolar integrated circuits, hybrids, biax, plated wire, or the more complex medium scale integration (MSI) and large scale integration (LSI) semiconductors.

The memory and memory sequencer built for the Nimbus-D VIP system utilizes discrete components, integrated logic circuits, and microbiax and core memories. In the advanced system, the designers elected to use MSI/LSI as much as possible. The three basic sections of the MAMS, containing memory, memory sequencer, and DC-to-DC converter-type power supply, are designed with multilayer boards connected vertically and hard-wired to interfacing connectors.

P-channel MOS integrated circuits were selected for memory and logic circuits because the specified bit-rate of the system is relatively low, and the need to conserve on power in a typical spacecraft or satellite environment is invariably high. Read-only memories were employed for several sequencer functions as well. Microprogramming techniques made it possible to replace large sections of control logic with LSI devices without the cost penalties of custom circuits. Section I, constituting the read-only portion of the MAMS, has a capacity of 512×10 words/bits, while Sections II and III provide for a 128×10 word/bit capacity. In effect, this offers the same capacity as the older and larger system used with the Nimbus-D satellite. Section II, the read/write memory which also has a nondestructive read-out (NDRO), requires only a few milliwatts of power. The new compact design enabled the use of a parallel mode for many internal memory sequencer functions, leaving the reprogrammer and formatter interfaces in serial mode. This increased the speed of the memory over the previous system and permitted substantial savings in logic formerly used to generate the shifting sequences.

2.4 Input/Output

Inputs to the memory sequencer include a 1.6 MHz clock code, commands for selecting one of the stored programs, plus certain control pulses. Flexibility is incorporated in the design by the provision for inputs to reprogram Section II with instructions or data different from those which were originally stored in the memory. The memory contains eight different sequences of instructions, each varying widely in complexity.

Outputs consist of address data, stored data (such as sync words) and major frame pulses (a frame consisting of a major division of the program being run). An output pulse advises as to the completion of a major frame with time varying according to the complexity of the program. Output of all information stored in the Memory is also possible, upon command.

2.5 Operation

The MAMS system, interfacing with a suitable information processor or multicoder, is capable of time-division multiplexing large quantities of data. The data capacity depends on the actual memory size and the type of format or program used. A typical example is the Nimbus-D system, which multiplexes 576 analog channels, 320 bilevel channels, 16 serial digital channels, and 1 time code channel.

The MAMS is block redundant, that is, the package actually contains two memories, two memory sequencers and two power supplies. Selection of block A or block B is done by external command. All critical circuits in the MAMS are current-limited, and all input signals are negative true to prevent damage to the memory from any open or partially open interfaces with the memory sequencer.

2.6 Summary

The results of the study conducted under the MAMS contract indicate it is technically feasible to reduce the size of the redundant memory and memory sequencer from three size 2/0 modules as developed for Nimbus-D VIP to one size 1/0 module. The size reduction is accomplished by employing semiconductor memories, LSI device techniques, and microprogramming. In addition, the expansion capability feature of VIP has been reduced, although the functional capability of the present VIP configuration is retained. The devices used are MOS P-channel for all memory circuits and most of the sequencer. Exceptions are DTL integrated circuits and discrete components used for buffers, power strobes, frame markers, and the DC/DC converters. The memory sequencer also utilizes three types of custom logic chips. Standard packaging techniques have been employed to provide a compression-loaded package with four multilayer printed wiring boards on which all electronic components are

mounted. The weight estimate is about 3.5 pounds. The estimated power dissipation of 1.2 watts is slightly higher than the design goal of one watt. However, it should be noted that this is a conservative estimate and will be affected by the final circuit design parameters.

3.0 MAMS PERFORMANCE CHARACTERISTICS

3.1 General Concepts

The purpose of the MAMS system is to provide a memory and memory sequencer unit which is electrically compatible with the existing Nimbus D VIP System, but in a significantly reduced volume from the original Nimbus D. This volume reduction is accomplished through the use of MSI and LSI techniques to replace large groups of logic functions with as few MOS chips as practical. Off-the-shelf MSI/LSI devices are used wherever possible to eliminate the high development costs of custom circuits. Where custom chips are necessary, the same device is used in as many applications as possible, thereby reducing the net cost per chip through increased quantity.

The mechanical design and electronics packaging techniques employed for the MAMS hardware design are basically the same as those used for the VIP System built for Nimbus D. The concept of a compression loaded stack has proven successful in previous Radiation designs and Radiation has gained considerable experience in the area of space-borne electronics. The design has been detailed to the fullest extent possible at the present time with consideration given to each of the following areas:

- Cost
- Dimensional Requirements of Electronic Components Using Latest Printed
Wiring Board Design Criteria
- Power
- Weight
- Environment
- Reliability

3.2 Design Goals

Paramount among the design requirements was to package the functional electronics for the memory and memory sequencer and electrical redundancy into a 1/0 size Nimbus module, maintaining weight below 4.0 pounds and the power level under 1 watt. Other goals were to maintain the flexibility of the present VIP and to increase the bit rate capability over the Nimbus design.

3.2.1 Priorities

Design priorities for the MAMS system as defined by NASA/Goddard are:

- a. Production cost
- b. Size - 1/0 Nimbus Module 2" x 6" x 6.5"
- c. Power - 1 watt maximum
- d. Development Cost
- e. Weight
- f. Flexibility
- g. Five years maintainability
- h. Production Schedule

3.3 Tradeoffs

Various tradeoffs were taken into consideration when developing the MAMS System. One such tradeoff was increasing the size of the main memory to reduce some of the control logic in the memory sequencer. This was not found to be very practical because it seriously limited the flexibility of the system, one of its outstanding features.

Another tradeoff considered was changing the redundancy scheme from cross-strapped memories and memory sequencers to block redundant units. This would eliminate the

need for two of the DC/DC converters and also significantly reduce the number of inter-board connections. Since the entire MAMS system is contained in a single box, and most data transfers are of a parallel nature, block redundancy was incorporated.

Magnetic memories and semiconductor memories were considered during the conceptual phase. Magnetic memories like microbiax and core, as used in VIP, require considerable amounts of peripheral electronics, such as decode gates, precision current drivers, and sense amplifiers. Plated wire offered some reduction in stack size over microbiax and core, but still needed all the surrounding electronics. As a result it was found that use of a magnetic memory would not allow sufficient space inside the MAMS box for the remaining memory sequencer logic, DC/DC converters, and major frame markers.

Semiconductor memories, on the other hand, have all the decode logic and sense amplifiers contained on the same chip as the storage devices. Therefore, a large, complete memory can be implemented with just a few flatpacks, and at less cost than an equivalent microbiax or plated wire system. As storage capacity per chip increases, and more vendors begin manufacturing memory devices, the cost per bit should be reduced even further making semiconductor memories more attractive.

3.4 Detailed Design Features

3.4.1 Functional Description

The basic MAMS operation is similar to the existing VIP in that a set of eight instructions is used to control the transfer of channel addresses, value data, and sync data from the main memory to the surrounding equipment. As in VIP, a large read-only memory is utilized in conjunction with a small scratch pad memory to generate commutated sequences by means of four stored programs. Also, all external interface signals from the VIP system have been retained. Differences within the MAMS unit consist of parallel data transfer rather than serial between the memory and the memory sequencer, and the use of microprogramming in the memory sequencer to generate various timing commands.

A block diagram of the MAMS system is shown in Figure 3.4.1-1 and VIP interface signals are shown in Figure 3.4.1-2.

3.4.1.1 Memory

3.4.1.1.1 Section I

Section I consists of a 512 word by 10 bit read only memory which is implemented with semiconductor ROMs. ROMs offer the advantage of a large amount of logic in a small package, with low power dissipation and at reasonably low cost. The disadvantage of an ROM memory for stored programs is, of course, inflexibility in changing the memory contents. However, of the three different vendors considered, each stated that new devices could be delivered six to eight weeks after obtaining the new program. This is considered to be acceptable for all except last minute changes.

A logic diagram of the memory is shown in Figure 3.4.1.1.1-1. After a ten bit address has been presented from the instruction counter, a read pulse enables the ROM output

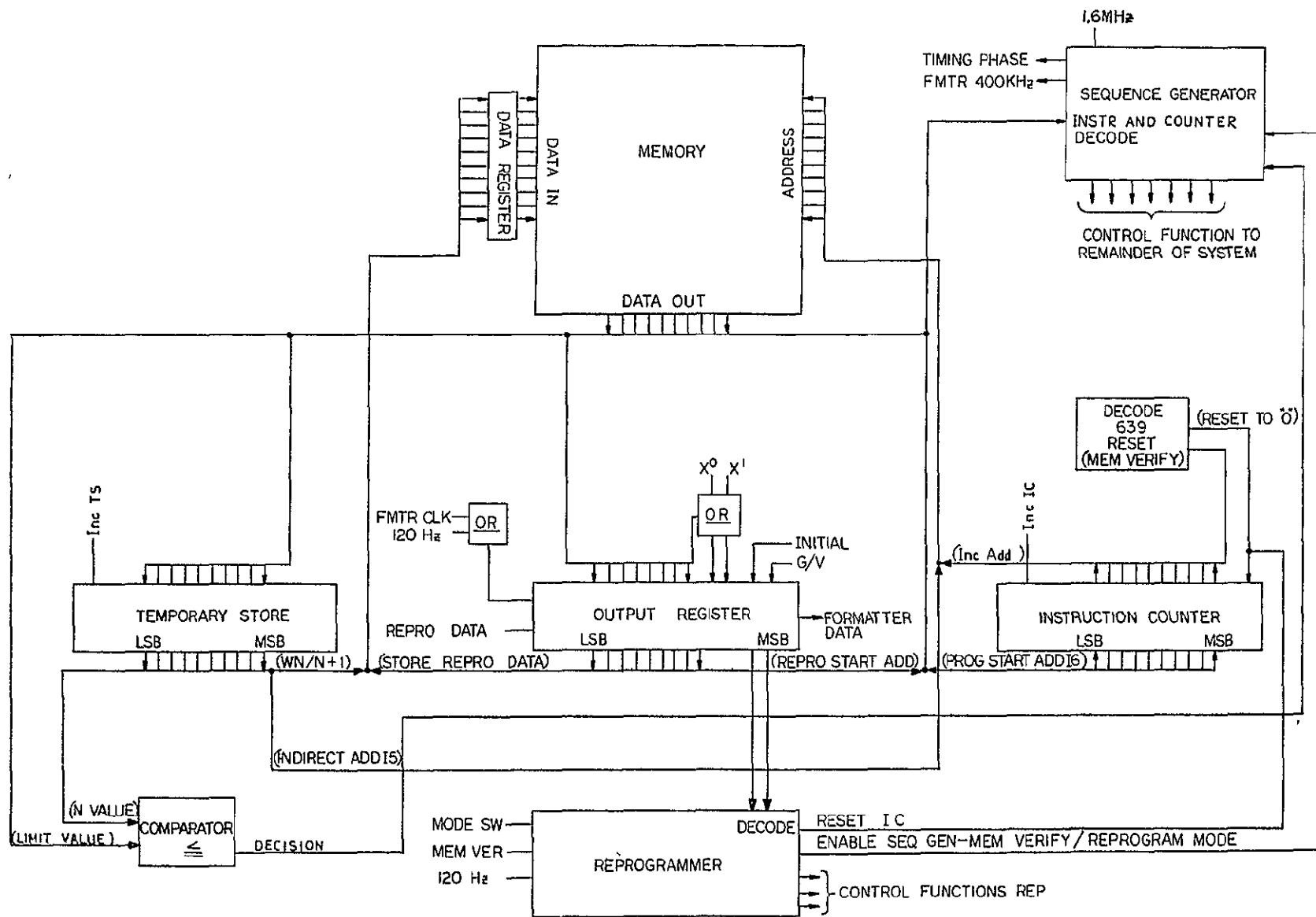


Figure 3.4.1-1
MAMS BLOCK DIAGRAM

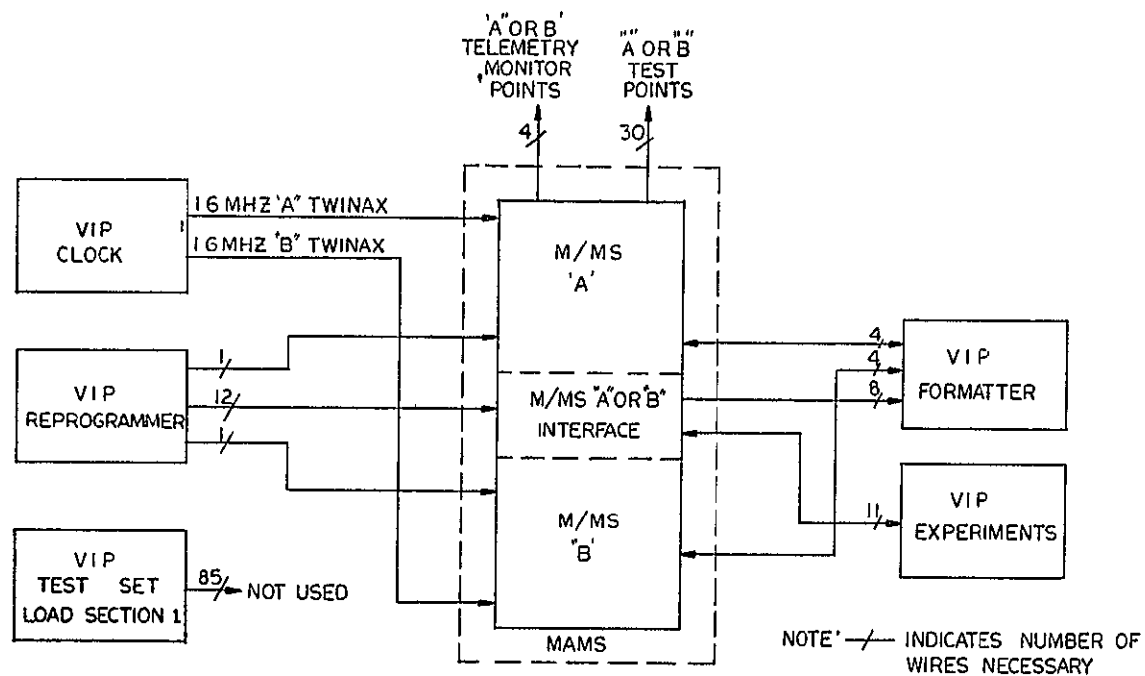


Figure 3.4.1-2

MAMS INTERFACE BLOCK DIAGRAM

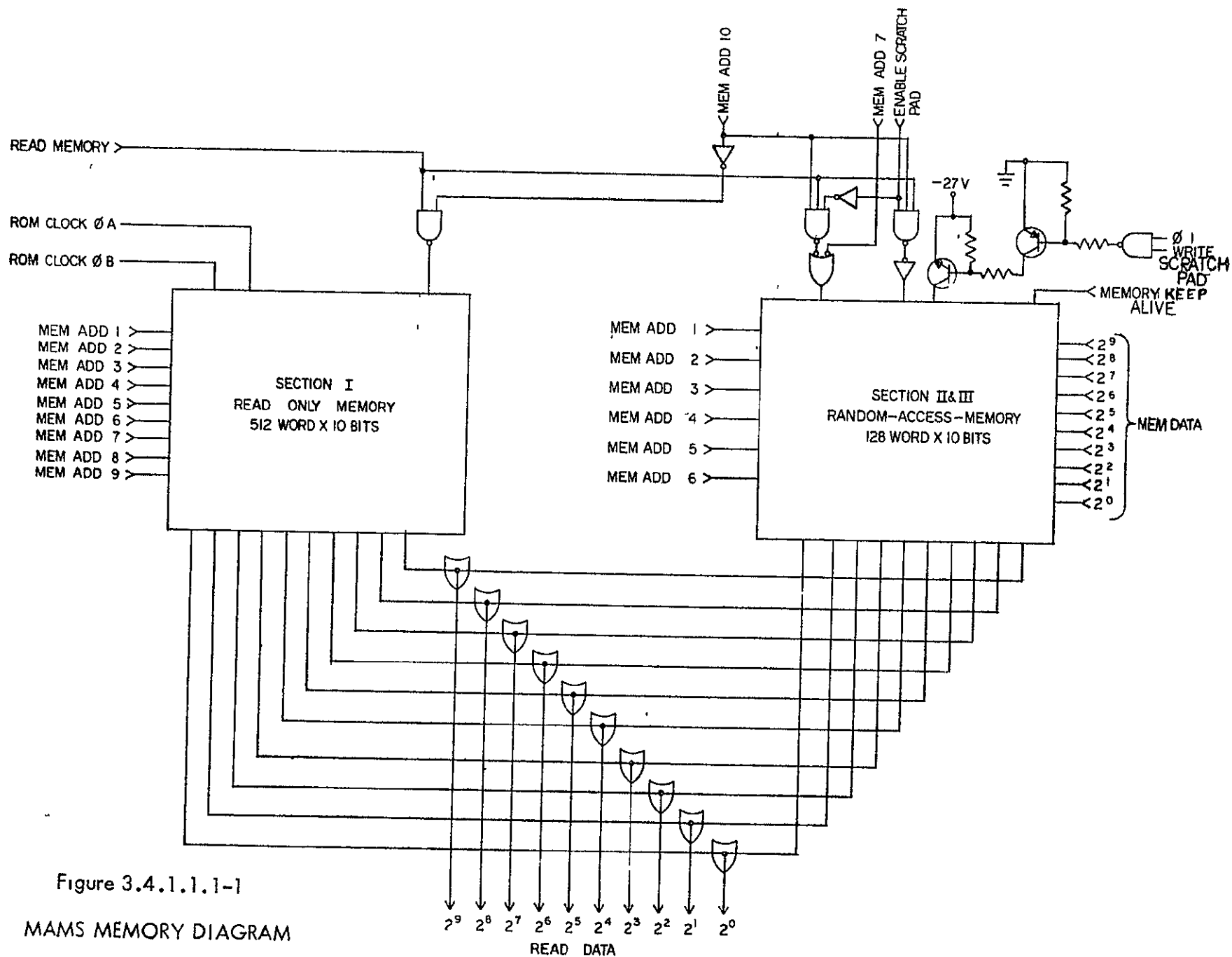


Figure 3.4.1.1.1-1
MAMS MEMORY DIAGRAM

drivers which in turn load the memory register (Figure 3.4.1.1.1-2). Data is only clocked into the memory register after sufficient time has elapsed to guarantee that the memory outputs have reached their proper level.

The device recommended for MAMS Section I is the Electronic Arrays 3500, a 512 word, 5 bits/word ROM which is packaged in a 24 lead flatpack. This device has output drivers and address decoding on the same chip as the memory matrix, and thereby offers very low power and small size. An output inhibit line is also made available so that the outputs of Section I may be wire - "OR"ed with the outputs of Sections II and III. As can be seen in Figure 3.4.1.1.1-1, the state of address bit 10 determines whether Section I or II will be enabled by a read command.

3.4.1.1.2 Sections II and III

Section II is a random access, read/write memory that stores a reprogrammable format. Since this section is required to have non-destructive, non-volatile outputs, special precautions must be taken if a semiconductor RAM is to be used. This is because of the nature of semiconductor memories, which use flip-flops as the storage element. If power is lost longer than the storage time of the device, information stored in the memory may be lost. To prevent such a power loss from transmitting bad data, a special power-fail detection circuit (Figure 3.4.1.2.6) has been added to the Section II power strobe. If, at any time, power is lost to Section II, a latch will be set and an override gate will prevent operation in Section II. In addition, the sequencer will jump back to a pre-determined format in Section I and a "power fail" level will appear at the Section II telemetry monitor point. The detection latch cannot be reset until Section II has been reprogrammed.

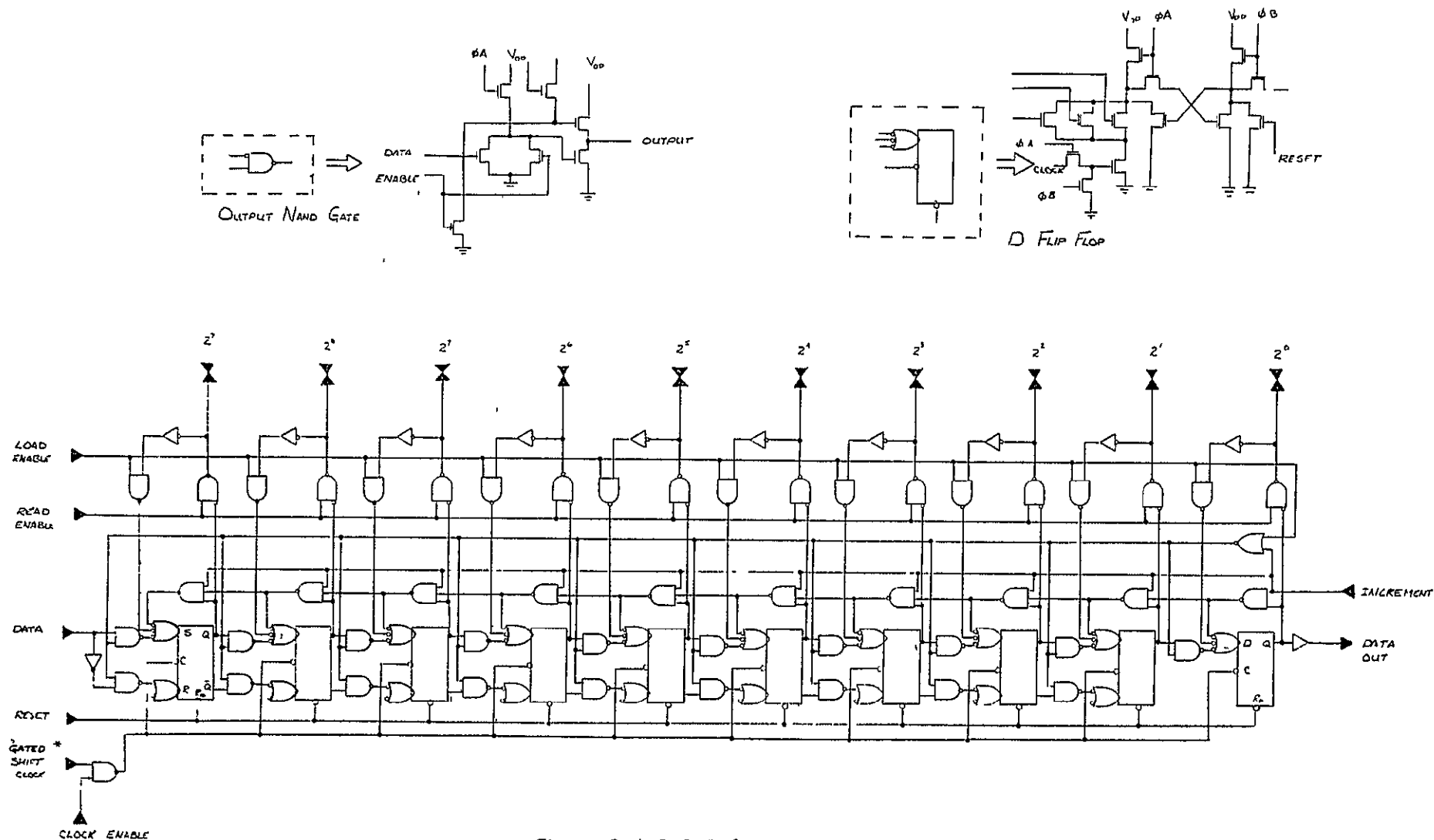


Figure 3.4.1.1.1-2

MAMS REGISTER LOGIC

*NOTE ALL REGISTERS CONNECTED TO GATED SHIFT CLOCK (400KHz) EXCEPT FOR OUTPUT REGISTER, WHICH CONNECTS TO FORMATTER CLOCK (100 KHz)

Section III requires only eight words by 10 bits with read/write capability. Since most RAMs are organized in a 64 word or 128 word matrix, it is more efficient to include Section III within the 128 words of Section II, leaving 120 words for Section II. Because VIP did not need the entire 128 words provided, it was felt that combining these two sections would be more advantageous from a space-saving standpoint than having excess words in Section III.

Section II gets its address from the instruction counter, as does Section I, and both Sections II and III enter data into the memory register (Figure 3.4.1.1.1-2) upon receiving the proper read command. The various clock phases for the memories are shown in Figure 3.4.1.1.2.

The Electronic Arrays EA1400, a 64 word x 2 bit RAM is used in the MAMS System for Sections II and III. This device has a feature which allows the user to turn off the main power to the flatpack when the element is not in use, yet maintain the information stored in the memory by means of a low power "keep alive" strobe. This reduces the average power dissipated by Section II to a low value because of the extremely low stand-by power required by the strobe.

3.4.1.2 Memory Sequencer

3.4.1.2.1 Sequence Generator

The MAMS makes use of a microprogrammer, or sequence generator, to generate the proper logic levels of all control signals at the correct time. This sequence generator consists of a large ROM which is partitioned into eight sections of 32 words each. Each of the eight sections corresponds to one of the eight instructions used to derive output data, and is programmed to carry out the sequential steps of the instruction as the address is incremented.

At the beginning of word rate, the sequence generator address register (Figure 3.4.1.2.1) is reset to zero. A 400 KHz clock then starts incrementing the sequence generator address register and commands are generated to increment the instruction counter and read the

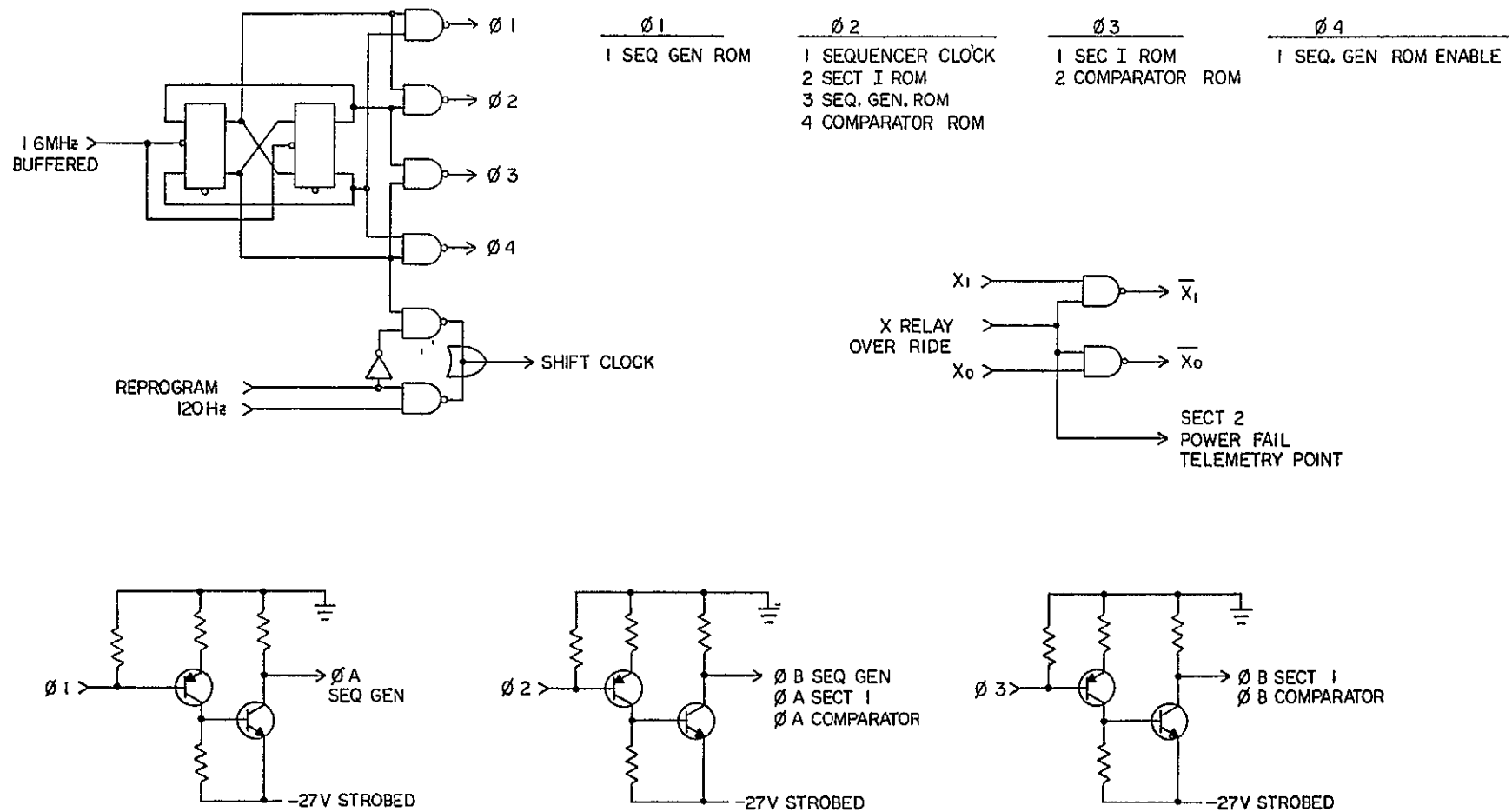


Figure 3.4.1.1.2
MAMS CLOCK CIRCUITS

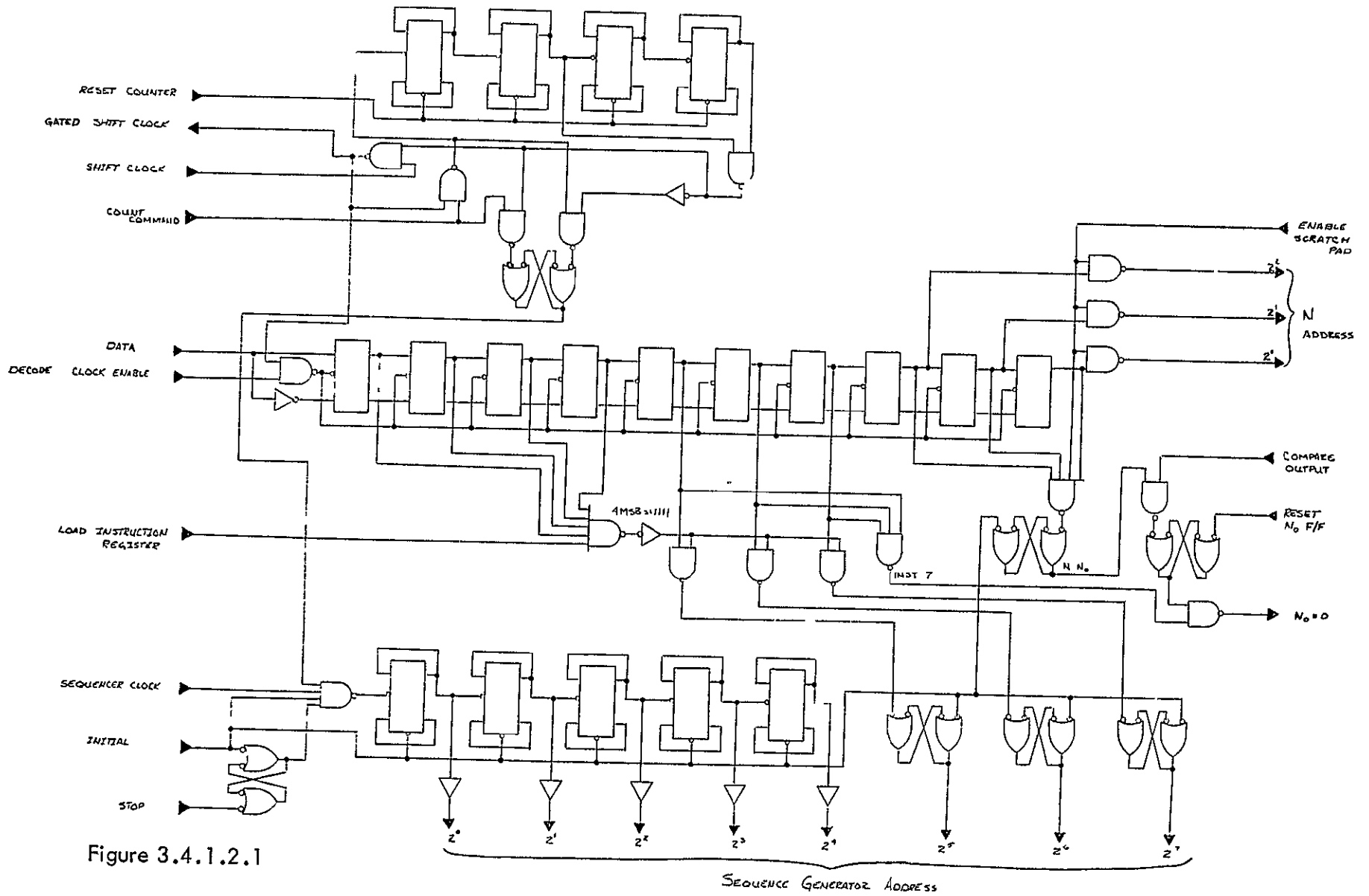


Figure 3.4.1.2.1

SEQUENCE GENERATOR ADDRESS REGISTER

memory. The memory data is then shifted to the sequence generator LSI chip (Figure 3.4.1.2.1) where the four most significant bits are decoded to determine whether there is an instruction or not. If the four MSBs are equal to ones, the fourth, fifth, and sixth bits (which define the instruction number) are shifted into the sequence generator address register which, in turn, addresses the proper portion of the sequence generator ROMs. The sequence generator address register continues to increment until the instruction has been carried out and a stop command is received.

A typical program is shown in the appendix. This approach of using ROMs to control the transfer and gating of data eliminates the need for several custom chips to provide the same functions. This means that the high development cost of custom circuits can be eliminated by replacing them with cheaper, off-the-shelf devices.

3.4.1.2.2 Instruction Counter

The instruction counter serves as the address register for the MAMS memory. It is another use of the multi-purpose register shown in Figure 3.4.1.1.1-2 and operates in the increment, parallel inparallel out modes as well as the serial-in mode. This register was designed to be used wherever a ten bit register was needed in MAMS, so as to reduce the number of different types of custom circuits. Other uses besides the memory registers and instruction counter are found below.

The instruction counter receives all its commands from the sequence generator and data may be loaded in from the X relays or from the formatter during reprogram.

3.4.1.2.3 Temporary Storage and Comparator

The temporary storage register also uses the register shown in Figure 3.4.1.1.1-2 and functions as a holding register for data that is to be written into the scratch pad (Section III).

Input and output enables are controlled by the sequence generator as they are for the other registers in MAMS.

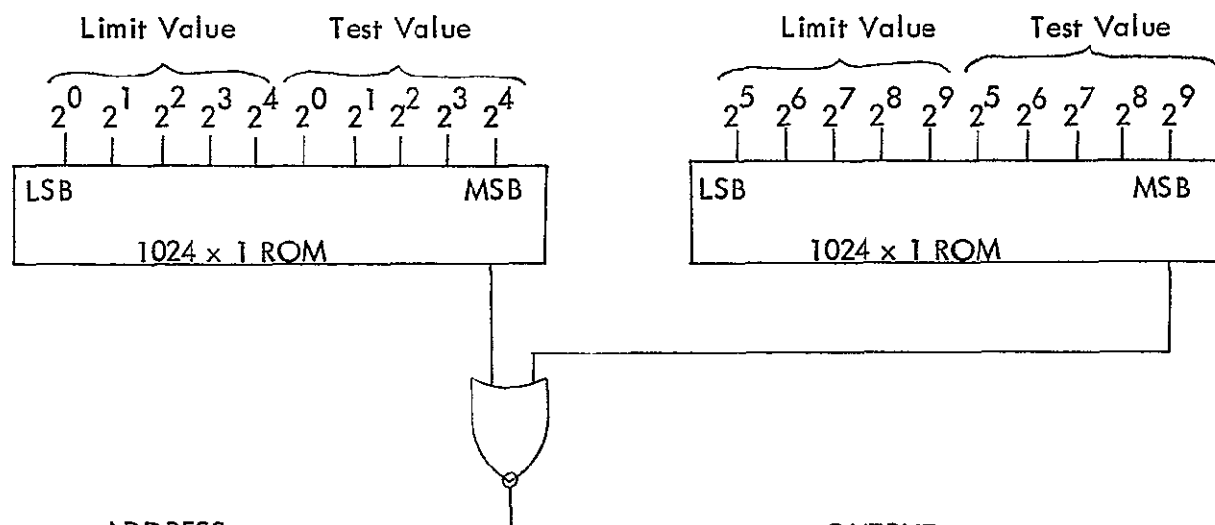
A second ten bit register is used to store the limit value during an instruction three or five. To perform a comparison between the limit value and the value currently held in temporary storage (the value of the N counter during this time slot), the outputs of the two registers are gated to the address lines of two 1024 X 1 ROMs, as shown in Figure 3.4.1.2.3. If the test value is equal to or greater than the limit value, then a compare value is present at the output of the ROMs. If the test value is less than the limit value, the temporary storage register receives an increment command from the sequence generator. This is followed by an output enable during which the newly incremented value is transferred to the memory data register and from there written back into the scratch pad.

3.4.1.2.4 Output Register

The output register is another application of the register in Figure 3.4.1.1.1.-2. The output register accepts parallel data from the memory register and shifts it out to the formatter serially. Two additional bits, the Gate/Value bit and the Multiplexer A/B bit are contained on the Reprogrammer LSI chip (Figure 3.4.1.2.4) and are shifted through the output register during the twelve bit formatter clock.

3.4.1.2.5 Reprogrammer

The reprogrammer logic is located on the third LSI chip, detailed in Figure 3.4.1.2.4. Initiation of the reprogram mode is effected by the memory sequencer when the mode switch signal from the Command Clock Subsystem changes to a logic one and the reprogram interlock signal is present. The reprogramming section of the memory sequencer logic generates a signal which inhibits operation of the memory sequencer for the duration of the reprogram



ADDRESS		OUTPUT
Test Value	Limit Value	(Test ≥ Limit)
MSB	LSB	
0 0 0 0 0	0 0 0 0 0	1
0 0 0 0 0	0 0 0 0 1	0
0 0 0 0 0	0 0 0 1 0	0
0 0 0 0 0	0 0 0 1 1	0
.	.	.
.	.	.
.	.	.
0 0 0 0 1	0 0 0 0 0	1
0 0 0 0 1	0 0 0 0 1	1
0 0 0 0 1	0 0 0 1 0	0
0 0 0 0 1	0 0 0 1 1	0
.	.	.
.	.	.
.	.	.
0 0 0 1 0	0 0 0 0 0	1
0 0 0 1 0	0 0 0 0 1	1
0 0 0 1 0	0 0 0 1 0	1
0 0 0 1 0	0 0 0 1 1	0
.	.	.
.	.	.
.	.	.
.	.	.

Figure 3.4.1.2.3

MAMS COMPARATOR

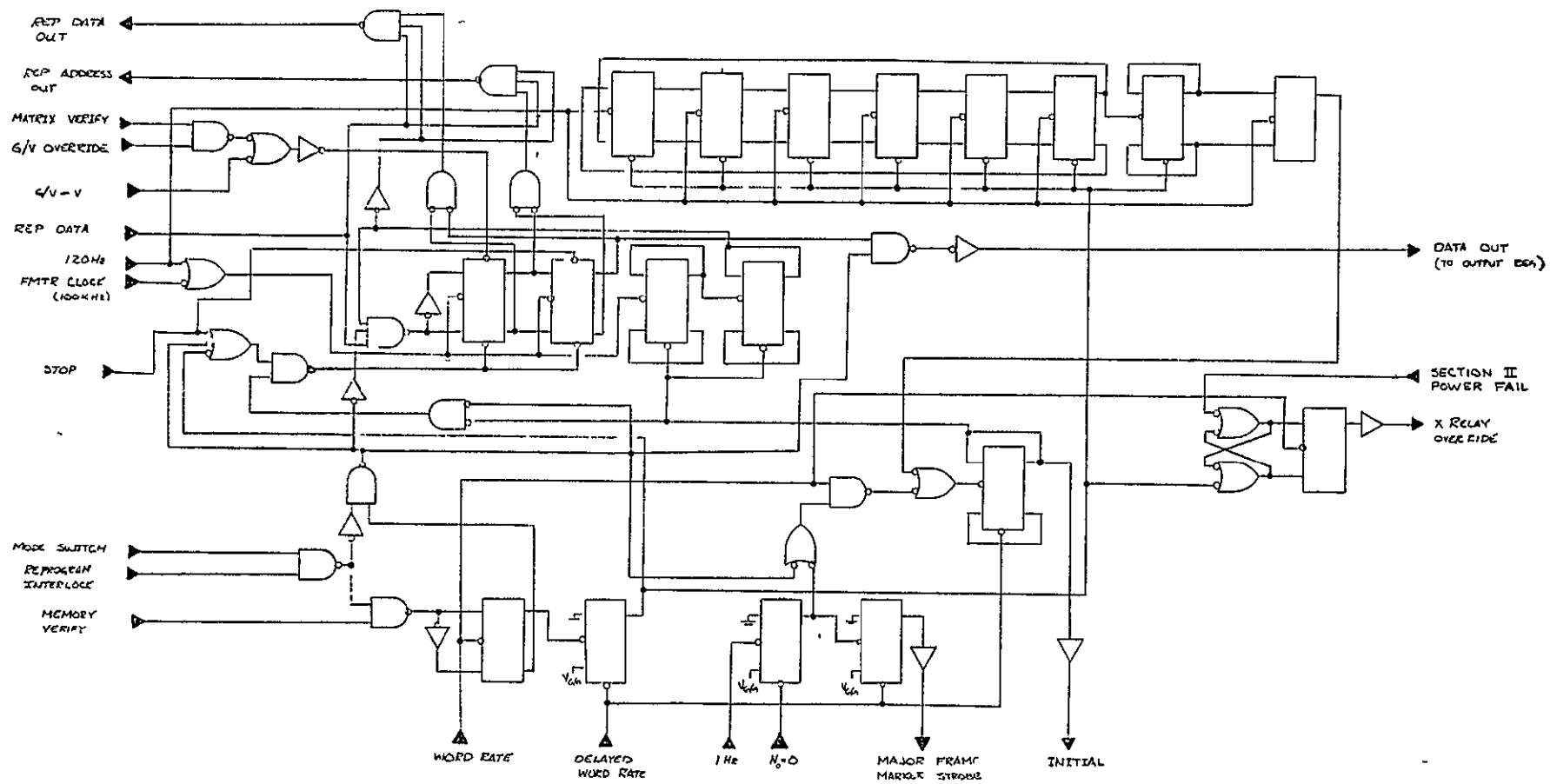


Figure 3.4.1.2.4

MAMS REPROGRAMMER LOGIC

cycle. If the memory sequencer is processing an instruction when the mode switch signal is received, this processing of the instruction is completed before operation of the memory sequencer is inhibited. The reprogram logic then accepts data and clock from the reprogramming unit. The first word received during a reprogram cycle is the starting address of a particular sequence and is routed to the instruction counter. The identification bits for the address word are 01, with 1 being the LSB. The address follows the ID with LSB first, and is one less than the actual starting address to be reprogrammed. All subsequent words are stored in memory at the appropriate memory location. Write commands and increment commands to the instruction counter are initiated by the sequence generator. Typical timing is shown in Figure 3.4.1.2.5.

Operation of the Memory Verify Mode, Matrix Verify Mode and Matrix Normal Mode is similar to the present VIP and descriptions of these modes can be found in the Supplemental Command Description referenced in the appendix of this report.

3.4.1.2.6 Discrete Circuits

Discrete circuits for the MAMS System consist of the DC/DC converters (one for each block redundant system), the memory "keep alive" circuit and power-fail detection, the major frame marker circuits, the input and output level shifters, and the various power strobes. The DC/DC converters and major frame markers are basically the same as in the VIP system. Output voltages of the converter have been adjusted to drive the high level P-channel MOS devices. The input and output level shifters are used to provide DTL interfaces for all signals entering and leaving the MAMS box. Typical level shifters are shown in Figure 3.4.1.2.6.

The ROMs and registers with the exception of the instruction counter and output register are power strobed to keep the system power dissipation as low as possible.

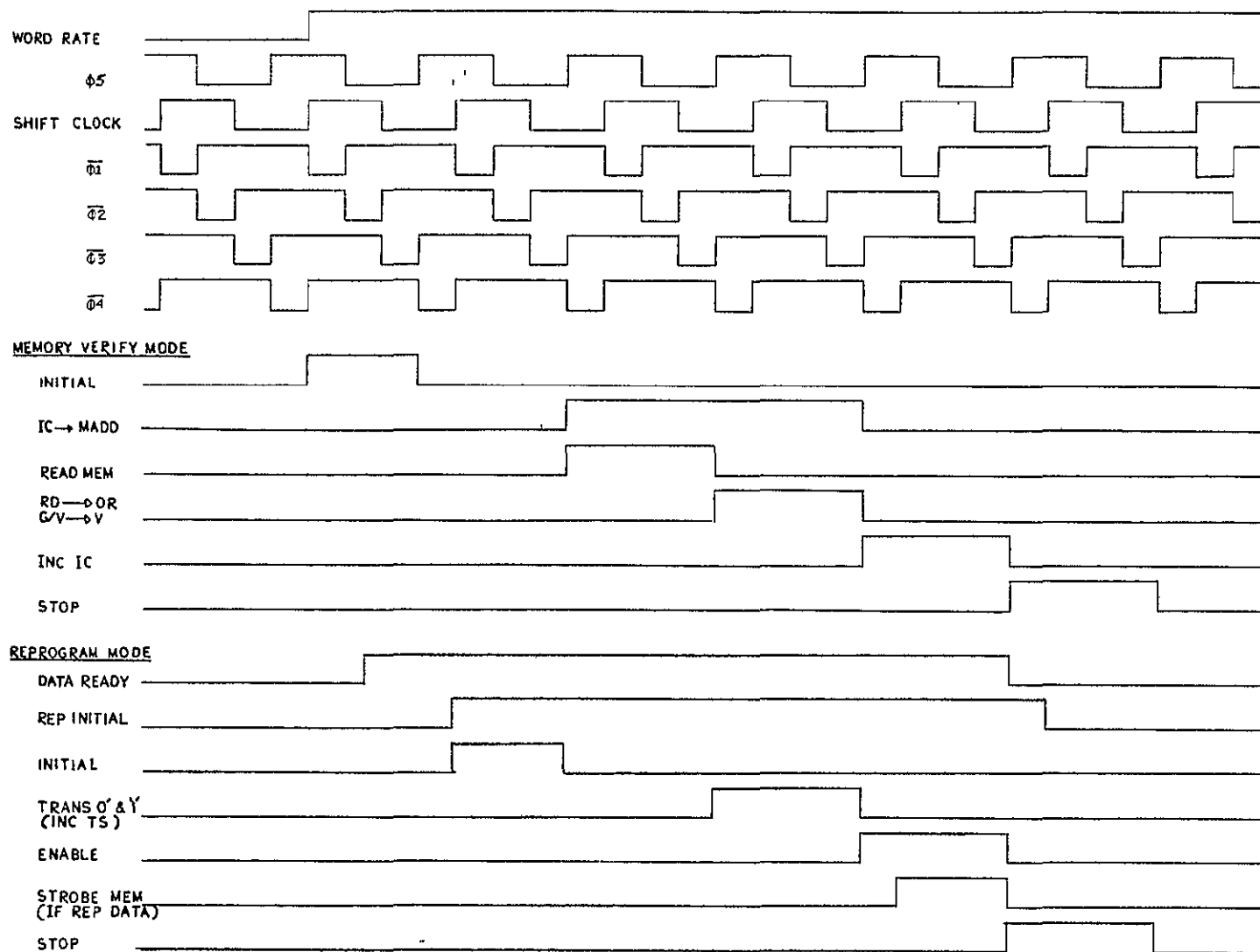


Figure 3.4.1.2.5

REPROGRAMMER TIMING DIAGRAM

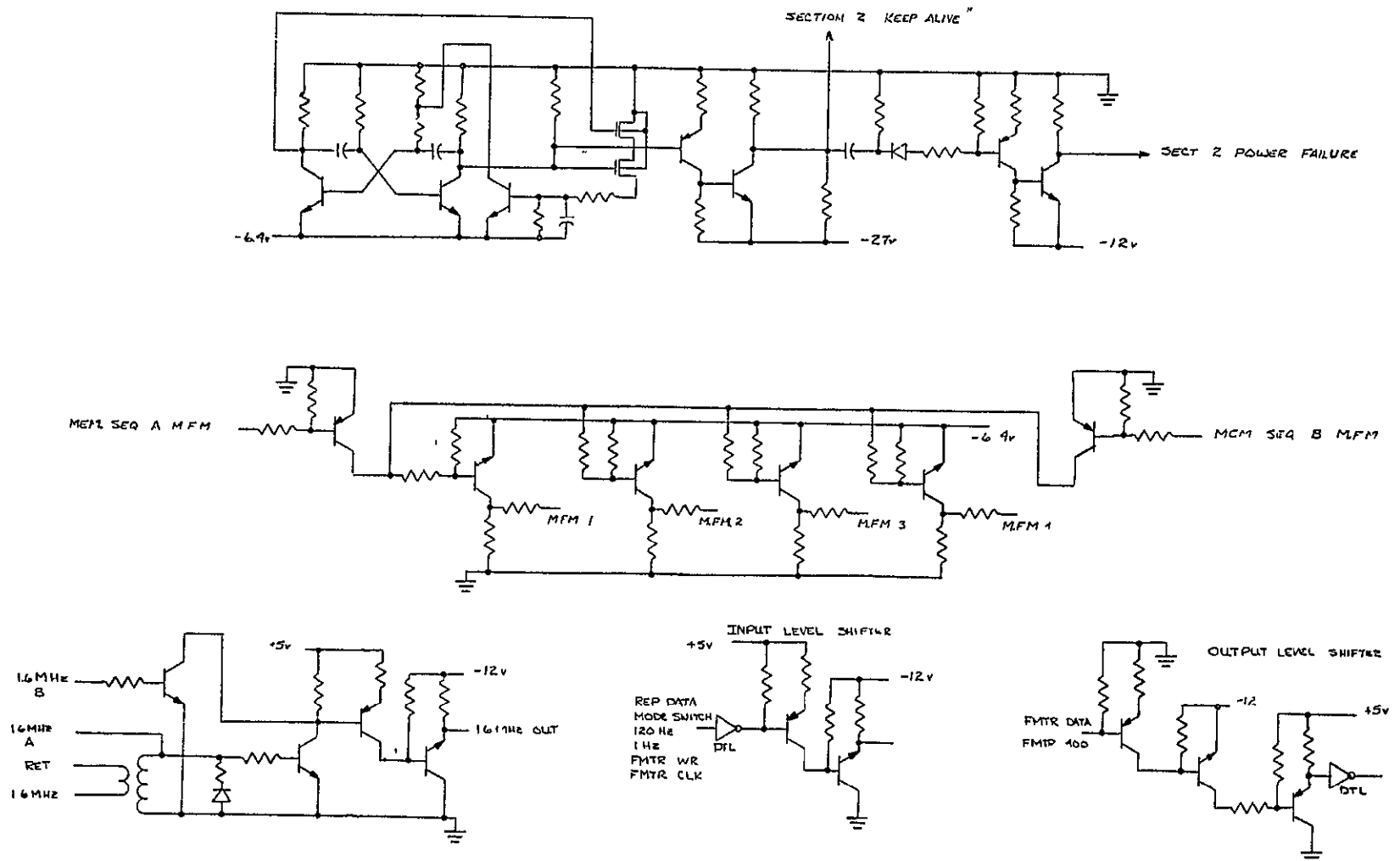


Figure 3.4.1.2.6

DISCRETE CIRCUITS

3.4.1.3 MAMS Instructions

The MAMS System uses the same set of eight instructions that were developed for the VIP. A complete description of each instruction can be found in the appendix and flow charts for each are shown in Figure 3.4.1.3.

3.4.1.4 MAMS Power

An estimate of the MAMS power dissipation is found below. This estimate is based on the use of dynamic high level p-channel logic devices with a clock rate of 400 KHz, and a power supply (DC/DC converter) efficiency of 75%. Most of the logic in the MAMS is power strobed and is only on for as long as it takes to complete an instruction. For purposes of the estimate below, an "on-time" of 100 usec was used. However, it should be noted that this represents a worst case time and that a majority of the instructions are much shorter. Therefore, the figure derived for the logic power is undoubtedly larger than the typical dissipation.

MAMS Power Calculation:

Registers

Dynamic F/F Duty Cycle 1/2

Dynamic Gates Duty Cycle 1/4

F/F Dissipation = 4 mw \times 1/2 = 2 mw ea.

Gate Dissipation = 2 mw \times 1/4 = 0.5 mw ea.

72 Gates \times .5 mw = 36 mw

10 F/F \times 2 mw = 20 mw

Total = 56 mw per register

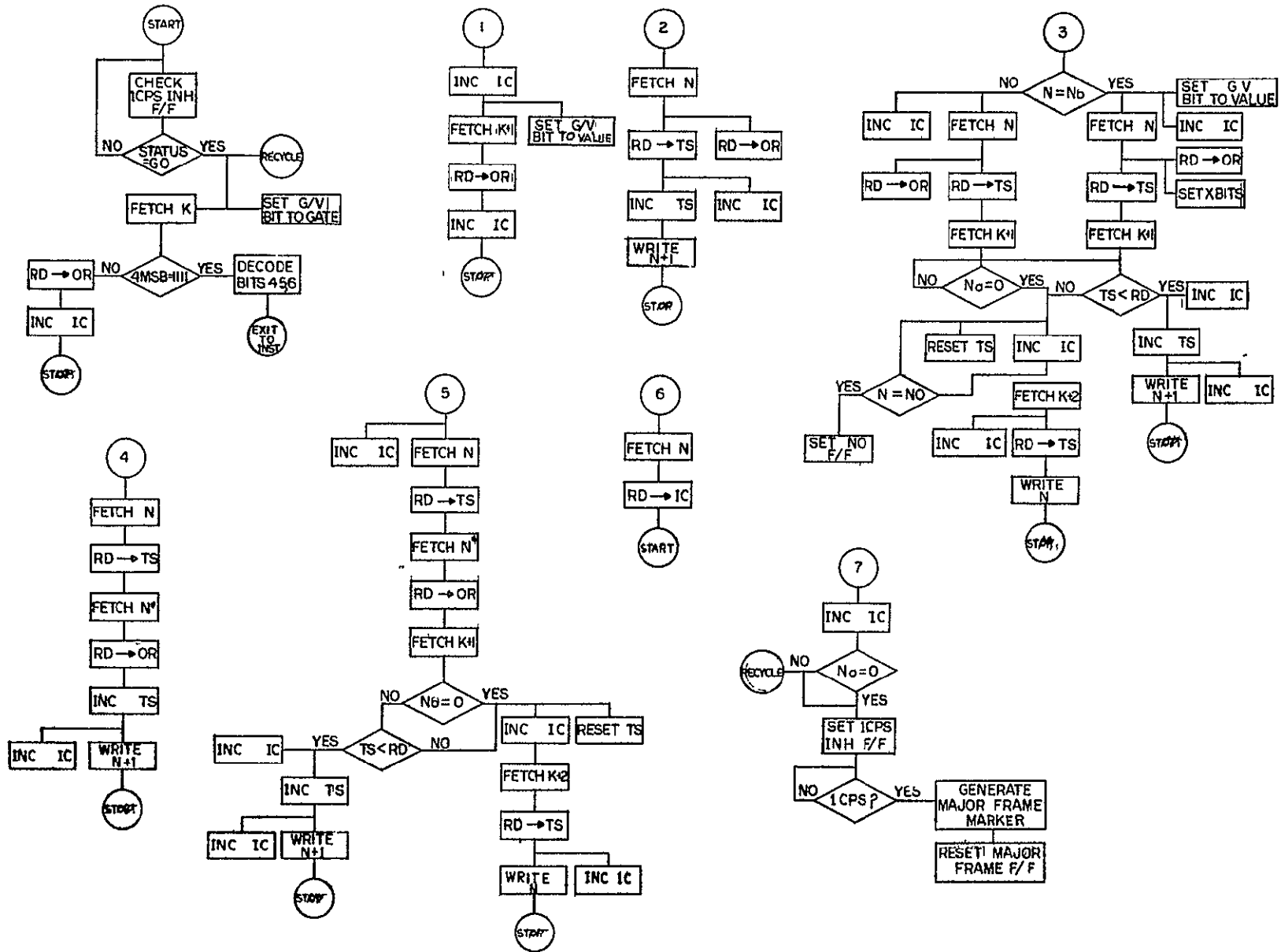


Figure 3.4.1.3

MAMS INSTRUCTION FLOW CHART

Reprogrammer Logic

$$30 \text{ Gates} \times .5 \text{ mw} = 15 \text{ mw}$$

$$18 \text{ F/F} \times 2 \text{ mw} = \underline{36 \text{ mw}}$$

$$\text{Total} = 51 \text{ mw}$$

$$\text{Ave} = 1/3 \times 51 = 27 \text{ mw}$$

Sequence Generator Address Logic

$$40 \text{ Gates} \times .5 \text{ mw} = 20 \text{ mw}$$

$$20 \text{ F/F} \times 2 \text{ mw} = \underline{40 \text{ mw}}$$

$$\text{Total} = 60 \text{ mw}$$

$$\text{Ave} = 1/3 \times 60 = 20 \text{ mw}$$

MAMS Power:

$$\text{Word Rate} = 3.2 \text{ KHz}$$

$$\text{Word Time} = 312 \text{ usec}$$

$$\text{Shift Time} = 120 \text{ usec}$$

$$\text{Operate Time} = 100 \text{ usec}$$

$$\text{Duty Cycle} = 100/312 = 1/3$$

Memory - Section I

$$\text{Clock Lines} = 32 \text{ mw} \times 2 = 64 \text{ mw}$$

$$V_{DD} \text{ Lines} = 6 \text{ ma} \times 12\text{v} \times 2 = \underline{144}$$

$$\text{Total} = 208$$

$$\text{Ave} = 1/3 \times 208 = 69 \text{ mw}$$

Memory - Section II - III

$$V_{GG} = 27v \times 3.2 \text{ ma} \times 10 = 865 \text{ mw}$$

$$V_{DD} = 12v \times .4 \text{ ma} \times 10 = \underline{48 \text{ mw}}$$
$$\text{Total} = 913 \text{ mw}$$

$$\text{Ave} = 1/3 \times 913 = 304 \text{ mw}$$

Instruction Counter

$$\text{Ave} = 1 \times 56 \text{ mw} = 56 \text{ mw}$$

Output Register

$$\text{Ave} = 1 \times 56 \text{ mw} = 56 \text{ mw}$$

Memory Register

$$\text{Ave} = 1/3 \times 56 \text{ mw} = 19 \text{ mw}$$

Temp. Storage Register

$$\text{Ave} = 1/3 \times 1/2 \times 56 \text{ mw} = 10 \text{ mw}$$

Comparator Register

$$\text{Ave} = 1/3 \times 1/10 \times 56 \text{ mw} = 2 \text{ mw}$$

Data Register

$$\text{Ave} = 1/3 \times 1/2 \times 56 \text{ mw} = 10 \text{ mw}$$

Comparator Memory

$$V_{DD} = 12v \times 12 \text{ ma} \times 2 = 288 \text{ mw}$$

$$V_{GG} = 27v \times 3 \text{ ma} \times 2 = \underline{162 \text{ mw}}$$

$$\text{Total} = 450 \text{ mw}$$

$$\text{Ave} = 1/3 \times 1/10 \times 450 = 15 \text{ mw}$$

Sequence Generator Memory

$$V_{DD} = 12v \times 4 \text{ ma} \times 4 = 192 \text{ mw}$$

$$\text{Clock Lines} = 16 \text{ mw} \times 4 = \underline{128 \text{ mw}}$$

$$\text{Total} = 320 \text{ mw}$$

$$\text{Ave} = 1/3 \times 320 = 107 \text{ mw}$$

Power Supply

DC/DC Converter Power
Consumption

$$\text{Max} = 300 \text{ mw}$$

Discrete Interfaces

$$5 \text{ mw} \times 20 \text{ Level Shifters} = 100 \text{ mw}$$

Memory "Keep Alive"

$$\text{Max} = 10 \times 4 \text{ mw} = 40 \text{ mw}$$

Major Frame Markers

$$\text{Max. Ave} = \underline{10 \text{ mw}}$$

$$\text{Total Discrete} = 450 \text{ mw}$$

Summary

$$\text{Ave Power Diss. of Logic} = 750 \text{ mw}$$

$$\text{Ave Power Diss. of Discretes} = \underline{450 \text{ mw}}$$

$$\text{Total Power} = 1.2 \text{ watts}$$

3.4.2 Electrical Components

3.4.2.1 Technology

Several different technologies are currently being developed in the MOS field.

The four most prevalent types now on the market are high level P-channel (both static and

dynamic), low level P-channel (static), and complementary symmetry. No one type seems to have a clear-cut advantage over the other, although new breakthroughs are changing the state-of-the-art almost daily. Complementary symmetry offers high speed and low power consumption; however, only one company is currently considered a source of these devices, and their output has been rather limited. Complementary symmetry is also substantially more expensive than the other three types. High level static devices have good speed characteristics and most MOS houses are actively producing this type of technology. The cost of high level static is relatively low compared to other types of MOS, however the power consumption is much greater.

High level dynamic logic and low level P-channel offer the best combination of speed, power consumption and cost. Of the two, the high level dynamic technology has been on the market longer and more vendors are currently equipped to manufacture it. However, increasing interest has been shown by the MOS vendors in the development of low level P-channel devices and improvements in the near future could give the low level technology a definite advantage over the others.

For the MAMS System it is recommended that the custom chips and any peripheral logic use high level dynamic P-channel technology. Because of the use of parallel data transfers within the MAMS, ultra fast shift clocks are not needed, thus enabling dynamic logic to offer a significant power saving. It must be noted, though, that the MAMS design is not limited to high level P-channel so that the same logic diagrams could also be used for low level chips if that type technology should become predominant. The term "low level" refers to low threshold voltage, usually two volts as opposed to five volts for high threshold logic. Before custom chips are actually produced it is recommended that a quick study of the existing market be undertaken for any major improvements in a certain technology.

3.4.2.2 Off the Shelf Devices

The MAMS System makes extensive use of off-the-shelf read-only memories and random access memories in an effort to reduce the amount of custom logic necessary. These devices are readily available from a large assortment of vendors and indications are that as the competition expands, the unit cost of each will drop. The various MAMS applications of off the shelf memories as described in Section 3.4.1 are: main storage memory (Sections I and II) and the scratch-pad memory (Section III), the sequence generator or microprogrammer, and the comparator. Several standard logic gates are used wherever the quantity of inputs prohibited inclusion in an LSI chip.

3.4.2.3 Custom Circuits

Because of the many special functions needed in the MAMS System, standardization of chip types to increase quantities was not as practical as in a less flexible system. However, the number of different LSI chip types was held to only three, one of which has numerous uses. The two chips that are not repeatable are the sequence generator address chip (Figure 3.4.1.2.1) and the reprogram logic chip (Figure 3.4.1.2.4). The third chip, a multi-function register (Figure 3.4.1.1.1-2) has several applications. It is used as the instruction counter, the memory register, the data register, the two temporary storage registers, and the output register.

Custom logic is expensive for systems such as MAMS because the large development costs are usually not amortized over large quantities. However, it is extremely efficient in terms of performance versus size, and the 2-inch height dimension specified for MAMS dictates use of such devices. Further study should be made in the area of size versus cost to determine whether a larger module (e.g. Nimbus 2/0), utilizing off-the-shelf devices rather than custom chips, would be more cost effective for a given application.

3.4.3 Mechanical Features

The proposed package assembly for the MAMS consists of four printed wiring board assemblies rigidly loaded into the 1/0 housing. The housing is constructed of magnesium and coated with electroless nickel, but an aluminum housing can be used at a sacrifice in weight if the 4 lb. weight limit is relaxed. The material is compatible with the structure of the Nimbus spacecraft. The proposed assembly design is depicted in Figure 3.4.3-1. The task initially causing most concern was front panel dimensional limitations for the Deutsch style connectors, but the panel has been redesigned to accommodate the desired electrical interface. Use has been made of as many existing VIP mechanical components as possible to conserve design and documentation costs and at the same time minimize the need for any additional prototype style tooling.

As another cost reduction technique, pre-molded polyurethane foam shims are used for card separation. A standard "window frame" configuration is used for all cards. The overall card stack dimension including a .060 inch foam spacer next to A4 solder fillets is determined to be 1.435 inch nominal before compression. Allowance for silicone rubber and epoxy shims is provided in order to bring the card stack up to the required compression loading.

The outline/interface dimensions can be seen in Figure 3.4.3-1, excluding the maximum connector projection of .509 inch past the unit mounting surface. Three 19-pin and one 44-pin Deutsch style connectors and 2 Twinax connectors were selected for the electrical interface and are distributed over the panel dimension as shown in the drawing.

Figure 3.4 3-2 shows the printed wiring board configuration with a card stack shim in position. The standard VIP printed wiring board is used.

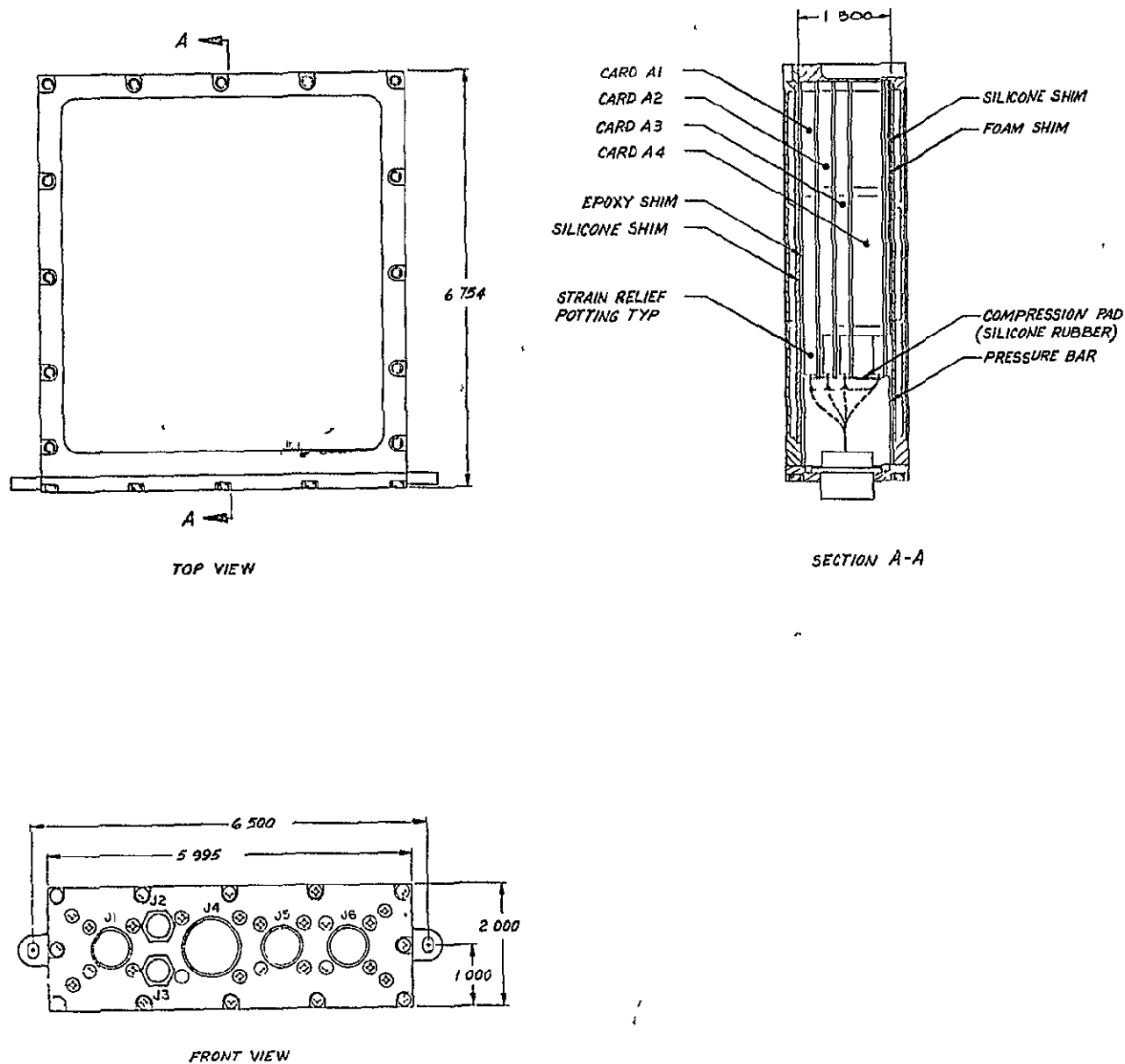


Figure 3.4.3-1
MECHANICAL DIAGRAM

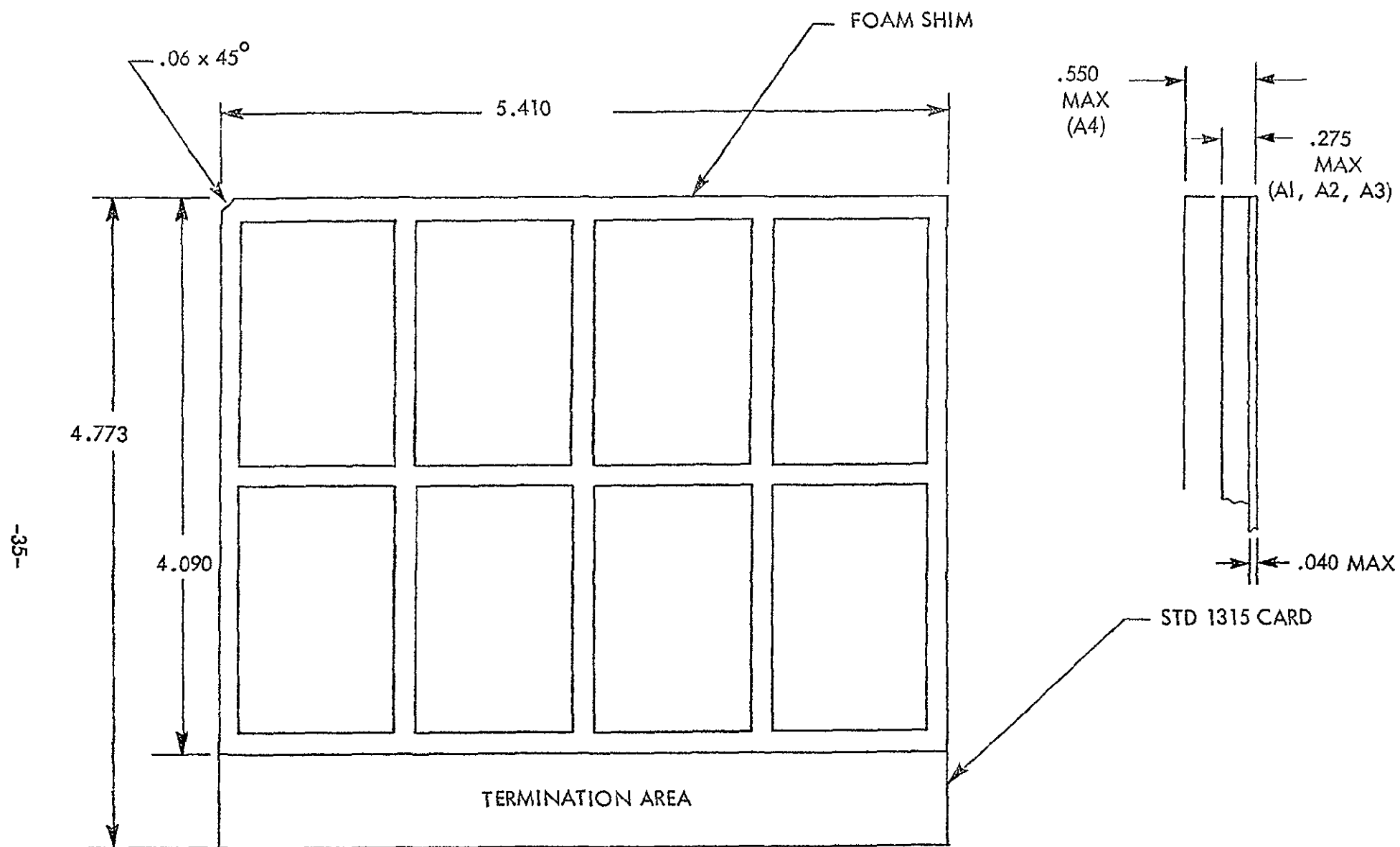


Figure 3.4.3-2

Interconnections are accomplished using multi-layer printed wiring techniques, with a minimum of 4 layers and a maximum of 8. All plated-through holes which have a lead installed in them and connections made on internal layers or located under a component are provided with an adjacent redundant plated-through hole with redundant connections made on the top, bottom, and internal layer which is used. Components are secured to the board using a conformal coating. The design layout criteria is essentially the same as that employed in VIP.

A1 and A2 are identical and contain memory and memory sequencer circuitry for blocks A and B. A representative layout is shown in Figure 3.4.3-3. Approximately 32 flat-packs are contained on each board, the exact number to be determined at time of partitioning. With a usable board area of 16.9 square inches, a 65 percent fill is calculated for each board.

A3 contains buffer, level shifter, clock failure, memory keep alive and 50 percent of the frame marker circuits. A 73 percent fill is calculated.

A4 contains two power supplies, strobe circuits and the remaining frame marker circuitry. A 77 percent fill is calculated. The magnetics used in the power supplies are located along the periphery of the board due to vibration considerations.

The weight of the unit is estimated to be 3.484 pounds and a summary of the estimated weight is given in Table 3.4.3. Also tabulated is the system weight if the choice is made to fabricate the housing from aluminum instead of magnesium.

3.4.4 Breadboard

3.4.4.1 Breadboard Design

The original concept of a breadboard for the MAMS study was to build a model of one of the LSI chips using small-scale integrated MOS devices. However, since the partitioning of the LSI chips was not expected to be completed in time to allow breadboard construction of a typical chip, it was decided that an abbreviated model of the MAMS System would be built.

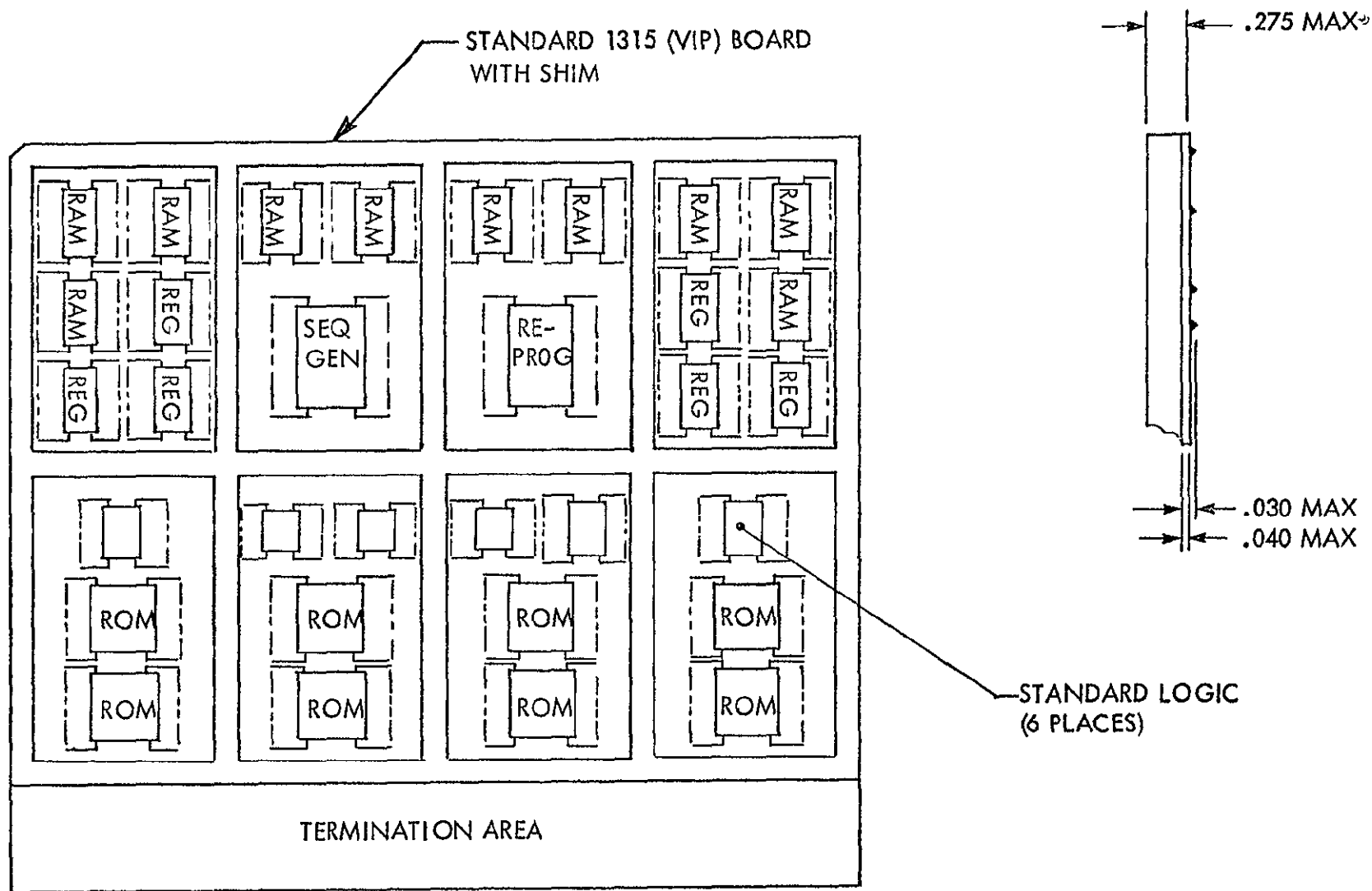


FIGURE 3.4.3-3

PRINTED WIRING BOARD ASSEMBLY (A1, A2)

MAMS
WEIGHT BREAKDOWN

Component	Estimated	Calculated	Actual
Housing			1.560 lbs
Top Cover			
Screws			
Front Panel/w Pressure Bars 2 Twinax Conn.			
3 CDS		.465 lbs	
P/S CD		.310 lbs	
3 Foam Shims			.106
1 P/S Shim			.112
1 ea. .060 Foam Shim			
2 ea. .032 Silicone Shim			
2 ea. Epoxy Shim			.078
24 Gauge Wire	.210 lbs		
4 Deutsch Conn.	.240 lbs		
WT RTV	.403 lbs		
	.853	.775	1.856

Total = 3.484 lbs (Mag)

24%	22%	54%
est.	cal.	Actual

Total Al = 4.294 lbs (Al)

TABLE 3.4.3

The breadboard constructed is capable of performing a series of instructions similar to those used in the MAMS System. Specifically, instructions zero, one, two, and six are implemented using a 64 word memory with 10 bit word length. Readout of information from the breadboard is performed by a DTL test fixture designed to simulate the VIP formatter interface.

3.4.4.2 Breadboard Parts

High level P-channel MOS devices were used in the breadboard because of their widespread availability and low cost. A ten bit shift register similar to the multi-function register in MAMS was also used, along with numerous logic gates and flip-flops. The use of MOS devices in the breadboard provided additional information as to what could be expected in the way of propagation delays, switching speeds, maximum clock frequencies, and power dissipation.

The memory elements used were the EA 1400's, the same devices projected for MAMS Memory Sections II and III. These units were found to have excellent noise characteristics and very low power dissipation in the standby mode.

3.5 Reliability

The following paragraphs present the reliability estimate for the final design configuration of the MAMS Study Program.

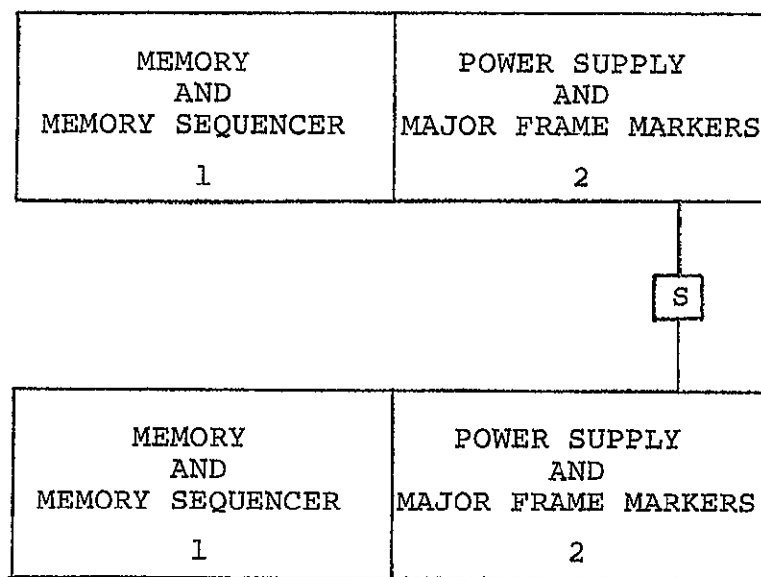
a. Goal

Design and reliability studies are directed toward achieving successful operations for one year in orbit, as specified for the VIP Subsystem.

b. Prediction Summary

The reliability of the proposed MAMS Subsystem is 0.9982 based on a one year mission time. Redundancy is used as shown in the Reliability Block Diagram of Figure 3.5 such that both the memory and memory sequencer are relay-switched by ground command. A math model, derived from the block diagram, is presented in Paragraph 3.5.1. A parts count summary is presented in Table 3.5 and a discussion of failure rates is contained in Paragraph 3.5.2.

For comparison, the reliability of a non-redundant system is 0.9589 considering screened parts as in the above prediction. The same configuration using non-screened parts has a reliability of 0.8827 considering redundancy and 0.6576 non-redundant. All calculations are based on the 1 year mission time.



RELIABILITY FOR ONE YEAR MISSION

	<u>SCREENED PARTS</u>		<u>NON-SCREENED PARTS</u>	
	<u>REDUNDANT</u>	<u>NON-REDUNDANT</u>	<u>REDUNDANT</u>	<u>NON-REDUNDANT</u>
1 -	-	0.9735	-	0.7649
2 -	-	0.9850	-	0.8597
TOTAL SUBSYSTEM	0.9982	0.9589	0.8827	0.6576

NOTE: Refer to Reliability Math Models

Figure 3.5

RELIABILITY BLOCK DIAGRAM

TABLE 3.5
PARTS COUNT SUMMARY PER BLOCK

<u>BLOCK SEGMENTS</u>	<u>PART TYPE</u>	<u>QTY (N)</u>	<u>FAILURE RATE $\lambda \times 10^{-6}$</u>	<u>$N\lambda \times 10^{-6}$</u>
Memory & Memory Sequencer	LSI	32	0.0480	1.5360
	Transistor			
	NPN	28	0.0195	0.5460
	PNP	12	0.0390	0.4680
	Diode	22	0.0195	0.4290
	Resistor, CC	86	0.00035	0.0301
	Capacitor, Cer.	6	0.0050	0.0300
	Transformer	1	0.0200	<u>0.0200</u>
			TOTAL	3.0591
Power Supply & Major Frame Markers	I.C.	7	0.0160	0.1120
	Transistor			
	PNP	2	0.0390	0.0780
	Diode	31	0.0195	0.6045
	Resistor, CC	48	0.00035	0.0168
	Capacitor, Tant	5	0.1700	0.8500
	Cer.	1	0.0050	0.0050
	Transformer	1	0.0200	0.0200
	Inductor	2	0.0200	<u>0.0400</u>
			TOTAL	1.7263

3.5.1 Reliability Math Models

Derivation of the expression used to represent the probability of successful operation for block redundant components whereby the active component fails at some time (t_1) and the standby component is switched into operation for the remaining time is presented in the following manner.

Success can be achieved in these ways:

- Components A and B succeed to time t (t is the mission duration).
- Component A fails at a time (t_1) which is less than t and component B must complete the operation. (The switching mechanism is assumed to work.)
- Component A succeeds to time t and the standby component B fails.

Translating these three conditions of success into time-independent probabilities results in.

$$R(t) = e^{-\lambda_A t} + \lambda_A e^{-\lambda_A t} \int_0^t e^{-(\lambda_A + \lambda_S)(t-t_1)} dt_1$$

where

λ_A = failure rate of the initially active component

λ_B = failure rate of the standby component

λ_S = failure rate of the switch

t = mission time

Solving the equation yields

$$R(t) = e^{-\lambda_A t} + \frac{\lambda_A}{\lambda_A + \lambda_S} e^{-\lambda_B t} [1 - e^{-(\lambda_A + \lambda_S)t}]$$

When the redundant components A and B have the same failure rate, this equation reduces to

$$R(t) = e^{-\lambda_A t} \left[1 + \frac{\lambda_A}{\lambda_A + \lambda_S} \left(1 - e^{-(\lambda_A + \lambda_S)t} \right) \right]$$

3.5.2 Failure Rates

Failure rates for all parts, with the exceptions noted below, were derived from MIL-HDBK-217A at 25°C temperature and minimum stress and were reduced by a factor of ten as specified in GSFC Specifications S-450-P-1A to reflect the quality improvement gained from part screening. An integrated circuit failure rate of 0.16×10^{-6} was established from data supplied by Texas Instruments.

A failure rate of 0.48×10^{-6} for LSI devices was derived for the detailed design review using the following rationale

MOS pin counts seem to be settling to 40 or less, which does not flirt too much with the dominant cause of IC failure, lead-bond damage and package ruptures. Forty leads are three times as many as a discrete IC flatpack, but since the circuit content is up at least 30:1, a 10:1 advantage per circuit function is gained. Thus, a failure rate for LSI flatpacks would be 3 times greater than the failure rate for discrete IC flatpacks.*

This failure rate is substantiated by data obtained from vendors that were surveyed as possible sources of LSI devices for the MAMS Subsystem. Results of the vendor survey are included in the Trip Report contained in the Appendix. It is concluded that failure rates for MOS devices will vary between 0.1×10^{-6} and 2×10^{-6} depending on complexity and size.

*Sideris, George, "The LSI Tradeoffs," Space/Aeronautics, March 69, p. 72.

4.0

APPENDIX

This Section of the report provides the following information:

- 4.1 Supplemental Command Description
- 4.2 Sequence Generator Sample Program
- 4.3 Trip Report - LSI Vendor Survey
- 4.4 AIMP Experience with MOS
- 4.5 Test Summary, Fairchild LSI

APPENDIX 4.1
SUPPLEMENTAL COMMAND DESCRIPTION
APPLICABLE TO VIP AND MAMS – NIMBUS SUBSYSTEMS

In the Versatile Information Processor subsystem, different internal commands as specified in Paragraph 3.4.1.2 of VIP Specification S-731-P-46 shall be used by the memory sequencer. These commands when executed in the proper sequence will be able to generate all of the types of programs or sequences required by the VIP Specification.

This Supplement provides a detailed description of a set of commands which meet the VIP Specification requirements and describes how these commands can be used to generate the sample format of Paragraph 3.4.1.3 of the VIP Specification,

I. DEFINITIONS

- 1) "K" refers to any 10-bit word memory location, other than a scratch pad word location, where a specific command is stored.
- 2) "K+1", "K+2", etc. refer to memory locations relative to a "K" location of a specific command.
- 3) "N" refers to any one of the eight scratch-pad 10-bit word memory locations. These eight locations are used as counters with the contents of one location, "N₀", assigned as the minor frame counter.
- 4) GATE/VALUE Tag refers to the memory sequencer output bit which specifies whether the 10-bit memory sequencer output is to be decoded by the formatting unit to select a particular data output (e.g., GATE) or whether the 10-bit output is to be inserted directly into the VIP output bit stream as sync, ID, etc. (e.g., VALUE).

- 5) "X" refers to 2 stored bits of information in the VIP which shall be used to specify the starting addresses of four programs which can be stored in memory. When "X" equals the binary counts of zero, one, two and three, the memory locations specified (addressed) shall be eight, nine, ten and eleven respectively. The "X" storage bits shall be controlled by four specific commands from the Nimbus Command Clock Subsystem. Two MSB's of No.
- 6) "Y" refers to any one of a maximum of 120 arbitrary memory locations used for indirect addressing.

II. MEMORY WORD DESCRIPTION

A memory word location shall contain 10 bit positions with the most significant bit in position #10, next most significant bit in position #9, etc. (least significant bit in position #1).

If the four most significant bits (e.g. bits #10, #9, #8, #7) of a memory word location are not all binary "ones" (e.g. "1111"), the entire 10 bit word shall be transferred to the memory sequencer output register (see "Command 0" of the following section).

If the four most significant bits of a memory word location are all binary "one's", the memory word shall be used to generate "Command 1" through "Command 7" (these commands are described in the following section). For these commands, bits #6, #5, and #4 of the memory word location shall be used to specify the command number with "001" specifying a "Command 1", "010" specifying a "Command 2", etc.; bits #3, #2, and #1 of the memory word location shall be used to specify any counter ("N") used with a command, with "000" specifying "N₀", "001" specifying "N₁", etc.

III. COMMANDS

At the initiation of each of the following commands, a different action is executed after first examining the contents of memory location "K".

After each command is executed, the memory sequencer output register shall not be changed until a "go" signal from the formatting unit is received. The "go" signal indicates that the formatting unit has stored and used for a sampling period the output register contents and the memory sequencer can begin executing the next command; in this manner, the memory sequencer generates addresses and values to the formatting unit at the proper rate to meet the required system sampling rates.

Unless otherwise specified only one command is executed during a VIP sampling period.

A. Command 0 Normal and Supercommutation

If "K" contains a "Command 0", transfer the contents of memory location "K" to the memory sequencer output register and set the output register GATE/VALUE Bit to GATE.

After a "Command 0" is executed, the next command shall be fetched from location "K+1".

A "Command 0" is used to generate sampling of arbitrary inputs one or more times in each minor frame.

Requires one word (10 Bits) memory storage for each time slot.

B. Command 1 Value

If "K" contains a "Command 1", transfer the contents of memory location "K+1" to the memory sequencer output register and set the output register GATE/VALUE tag to VALUE.

After a "Command 1" is executed, the next command shall be fetched from location "K+2".

A "Command 1" is used to generate synchronization, identification and other VALUE words.

Requires two words (10 Bit each) of memory storage for each (1)word (10 Bits) of Sync or ID word.

C. Command 2 Sequential Subcommutation W/O Limits

If "K" contains a "Command 2", transfer the contents of the specified scratch-pad memory location "N" to the memory sequencer output register, set the GATE/VALUE tag to the GATE, and then increment the contents of "N" by the binary count of one.

After a "Command 2" is executed, the next command shall be fetched from location "K+1".

A "Command 2" is used with a "Command 3" to generate sequential subcommutation sequences (e.g.....input 5, input 6, input 7, input 8). A "Command 3" must be used to specify the starting and limit values each sequential subcommutated sequence.

D. Command 3 Sequential Subcommutation with Limits

If "K" contains a "Command 3", transfer the contents of the specified scratch-pad memory location "N" to the memory sequencer output register. If "N" specifies " N_0 " (the minor frame counter), transfer the contents of "X" to the two most significant bit positions of the memory sequencer output register and set the GATE/VALUE tag to VALUE. (It is noted that " N_0 " shall be limited to a maximum binary count of 255 (8 bits). Therefore, for " $N=N_0$ " only, 8 not 10 bits shall be transferred to the low order positions of the memory sequencer output register). If "N" specifies any counter other than " N_0 " set the GATE/VALUE tag to GATE.

Next check " N_0 " to determine if " N_0 " equals the binary count of one. (This check is not made when the "N" specified by the "Command 3" in "K" is " N_0 " since the purpose of this check is to make the other "N" counters synchronous with " N_0 ".)

A count of one in " N_0 " indicates that the minor frame being generated is the first minor

frame of the major frame. If the contents of " N_0 " equals the binary count of one, then load "N" with the contents of " $K+2$ ". If the contents of "N" are equal to or greater than the contents of " $K+2$ ". If the contents of " N_0 " does not equal one, proceed with the following test which is also performed when the "N" specified by the "Command 3" in "K" is " N_0 ".

Test the contents of "N" against the contents of " $K+1$ ". If the contents of "N" are less than the contents of " $K+1$ ", then increment the contents of "N" by a binary count of one. (" $K+1$ " shall contain the limit value of the sequence.) If the contents of "N" are equal to or greater than the contents of " $K+1$ ", then load "N" with the contents of " $K+2$ ". (" $K+2$ " shall contain the starting value of the sequence.)

After a "Command 3" is executed, the next command shall be fetched from location " $K+3$ ".

A "Command 3" is used with a "Command 2" to generate sequential subcommutation sequences. A "Command 3" must be used to specify the starting and limit values for each sequential subcommutated sequence. This command also generates the minor frame count and program mode identification word.

E. Command 4 Arbitrary Subcommutation W/O Limits

If "K" contains a "Command 4", use the contents of the specified scratch-pad memory location "N" to select (indirectly address) a "Y" word to the memory sequencer output register, set the GATE/VALUE tag to GATE and increment the contents of "N" by one.

After a "Command 4" is executed, the next command shall be fetched from location " $K+1$ ".

A "Command 4" is used with a "Command 5" to generate arbitrary subcommutation sequences (e.g.....input 5, input 14, input 81, input 7.....). A "Command 5" must be used to specify the starting and limit "Y" addresses for each arbitrary subcommutated sequence.

F. Command 5 Arbitrary Subcommutation with Limits

If "K" contains a "Command 5", use the contents of the specified scratch-pad memory location "N" to select (indirectly address) a "Y" memory location, and then transfer the contents of "Y" to the memory sequencer output register and set the GATE/VALUE tag to GATE. (It is noted the "N₀" would never be specified by a "Command 5".)

Next check "N₀" to determine if "N₀" equals the binary count of one. (The purpose of the check is to make the other "N" counters synchronous with "N₀".)

A Count of one in "N₀" shall indicate that the minor frame being generated is the first minor frame of the major frame. If the contents of "N₀" equals the binary count of one, then load "N" with the contents of "K+2". If the contents of "N₀" does not equal the binary count of one, proceed with the following test:

Test the contents of "N" against the contents of "K+1". If the contents of "N" is less than the contents of "K+1", then increment the contents of "N" by a binary count of one. ("K+1" shall contain the limit address of the sequence.) If the contents of "N" is equal to or greater than the contents of "K+1", then load "N" with the contents of "K+2". ("K+2" shall contain the starting address of the sequence.)

After a "Command 5" is executed, the next command shall be fetched from location "K+3".

A "Command 5" is used with a "Command 4" to generate arbitrary subcommutation sequences. A "Command 5" must be used to specify the starting and limit addresses for each arbitrary subcommutated sequence.

G. Command 6 Jump

If "K" contains a "Command 6", examine the contents of " N_0 ". If the minor frame count indicates the last minor frame of the major frame (e.g. contents of " N_0 " equals the binary count of zero), examine "X" and then load the instruction counter with the contents of the memory location specified (addressed) by "X". If the minor frame count does not equal the binary count of zero, load the instruction counter with the contents of "K+1" which shall specify the starting address of the program being executed.

It is noted that both the command following a "Command 6" and the "Command 6" are executed during a VIP sampling period.

After a "Command 6" is executed, the next command shall be fetched from the location specified by the instruction counter.

A "Command 6" is used to either jump back to the starting point of the program being generated or to jump to the starting point of a new program such that the new commutation sequence (program) always begins at the start of a major frame.

H. Command 7 Synchronization

If "K" contains a "Command 7", examine the contents of " N_0 ". If the contents of " N_0 " equals the binary count of zero, execute the next command which shall be in location "K+1". (This command will normally be a "Command 1" used to generate the minor frame sync word.) After this command in "K+1" is executed, do not proceed with the execution of another command until the VIP one per second synchronization

pulse from the formatting unit is accepted by the memory sequencer.

If the contents of " N_0 " does not equal the binary count of zero, execute the next command which shall be in location " $K+1$ ". The check of the VIP one per second synchronization pulse is not required when " N_0 " does not equal binary count of zero.

It is noted that both the command following a "Command 7" and the "Command 7" are executed during a VIP sampling period.

After a "Command 7" is executed, the next command shall be fetched from location " $K+1$ ".

A "Command 7" is used to make the memory sequencer and the formatting unit timing synchronous with the Nimbus D Command Clock subsystem which generates the primary spacecraft clock frequencies and the Minitrack Time Code. If the memory sequencer and the formatting unit timing are synchronous with the Command Clock, the execution of a "Command 7" shall have no effect on the output program being generated by the memory sequencer; however, if the VIP is not in synchronism or loses synchronization with the Command Clock, execution of a "Command 7" by the memory sequencer shall "halt" generation of the memory sequencer program until synchronization is established.

MODE CHANGE RESPONSE

Gate Value Bit to Value

When the gate value bit is set to value the value flip flop in the output register is set and all subsequent words applied to the Formatter have the gate/value bit set. The gate/value bit is prevented from setting during the time the formatter is shifting the data out (which is the only time a clock is applied to the gate/value flip flop). Thus, if the command is received before the shift clock from the formatter, the change over from gate to value will occur during that particular word time; however, if the command is received after the formatter shift clock, the change from gate to value occurs at the next word. For example, let us suppose we are at time slot 20 (in the memory sequencer) and the gate/value to value command is received before the formatter shift clock, then the word which is associated with time slot 20 will have the gate value bit set. Now, if the command is received during time slot 20 but during or after the formatter shift clock, time slot 21 will contain the first value word.

Gate Value to Gate

When the gate value bit to gate command is received (and the bit is currently set to value) the change over is performed in a manner analogous to the gate value to value mode change.

Verify Memory

When the memory dump command is received the memory sequencer reads the entire contents from location 0 to location 639 and transfers the contents of each location to the formatter. This is repeated for as long as the command is in the true state. If the memory sequencer is processing an instruction, it finishes processing that instruction

Verify Memory (Cont'd.)

before initiation of the memory dump. The first location to be dumped is location 1.

When the memory dump command is removed, the memory sequencer will execute an instruction six and commence operation at the beginning of the specified program.

Normal operation of the memory sequencer is inhibited during the memory dump and the gate/value bit is forced to value.

Mode Switch (Reprogram Mode)

When the mode switch goes true, the reprogramming section of the memory sequencer logic generates a signal which inhibits operation of the memory sequencer for the duration of the reprogram cycle. If the memory sequencer is processing an instruction when the mode switch signal is received, this processing of the instruction is completed before operation of the memory sequencer is inhibited. The reprogram logic then accepts data and clock from the reprogramming unit. The first word received during a reprogram cycle is the starting address of a particular sequence and is routed to the instruction counter. The identification bits for the address word are 01, with 1 being the LSB. The address follows the ID bits with LSB first. For example, if the starting address was 513 the word would appear as 100000000101, with the ID bits to the right. The starting address is one less than the actual initial address to be reprogrammed. All subsequent words are stored in memory at the appropriate memory location. The identification bits for the data words are 10, with 0 being the LSB. The data follows the ID bits with LSB first. For example, if the data was 525 the word would appear as 010101010110 with the ID bits to the right. If a new starting address is received during a reprogram cycle, the memory sequencer will store the following word in the appropriate address and all subsequent words at their respective addresses. Upon the termination of the reprogramming

Mode Switch (Reprogram Mode) (Cont'd)

cycle by either the loss of the mode switch signal or the reprogrammer interlock signal, the memory sequencer will execute an instruction six and commence operation at the beginning of the specified format. During the reprogram cycle the formatter utilizes ten stages of its eleven stage counter (the eleventh stage is disabled in the Nimbus D configuration) to obtain addresses. These addresses are functionally broken down as shown below.

<u>Address</u>	<u>Function</u>
0 thru 15	Digital A Data
16 thru 31	Random Data
32 thru 63	Digital B Data
64 thru 639	Analog Data
640 thru 895	Analog Expansion (Output Zeroes)
896 thru 958	Random Data
959	Time Code
960 thru 1023	Value Data

Memory Write/Memory Sequencer Inhibit

The true state of the reprogrammer interlock signal enables the memory sequencer to go into reprogram mode upon receipt of the mode switch signal. Thus, receipt of the mode switch signal when the reprogrammer interlock signal is absent has no effect on the memory sequencer. If the reprogrammer interlock signal is removed while the reprogram logic is in operation it will interrupt operation of the reprogram cycle and cause the memory sequencer to execute an instruction six and return to the beginning of the specified format.

X Code

Initiation of a new format is accomplished by commanding the relays which generate the X code (X_0 , X_1). The memory sequencer will then switch to the new format at the end of the current minor frame during the execution of an instruction six. If the X code relays are commanded while the memory sequencer is reading the X code, there is a slight possibility that the first minor frame after the selection of the new format will be in error. This can occur if the relays are commanded within 250us of the leading edge of MAMS word rate when executing an instruction six.

X Code Override

This command forces the memory to format 1 (memory location 16) at the end of the current minor frame. Since this command forces the X_0 , X_1 inputs to the ground state, the memory sequencer cannot distinguish between this command and a normal format 1 ($X_0 = 0$, $X_1 = 0$) command.

APPENDIX 4.2

SEQUENCE GENERATOR SAMPLE PROGRAM

SEQUENCE GENERATOR
SAMPLE PROGRAM

SEQUENCE GENERATOR
ADDRESS

Inst. Reg			
000			
00000			
00001			
00010			
00011			
00100			
00101			
00110			
00111			
01000			
001			
00101			
00110			
00111			
01000			
01001			
01010			
01011			

Jump

Instruction Ctr. Increment
Instr. Ctr. Shift Clk. Enable
Instr. Ctr. Read Enable
Instr. Ctr. Load Enable
Instr. Ctr. Reset
Memory Reg. Shift Clk.
Mem. Reg. Read Enable
Mem. Reg. Load Enable
Mem. Reg. Reset
Data Reg. Shift Clk.
Data Reg. Read Enable
Data Reg. Load Enable
Data Reg. & Output Reg. Reset
Output Reg. Shift Clk.
Output Reg. Load Enable
Temp. Store Increment
Temp. Store Shift Clk.
Temp. Store Read Enable
Temp. Store Load Enable
Temp. Store & Compare Reset
Load Instr. Reg.

[illegible]

SEQUENCE GENERATOR ADDRESS	Inst. Reg	
	010	011
Instruction Ctr. Increment		1
Instr. Ctr. Shift Clk. Enable		1
Instr. Ctr. Read Enable		1
Instr. Ctr. Load Enable		1
Instr. Ctr. Reset		1
Memory Reg. Shift Clk.		1
Mem. Reg. Read Enable		1
Mem. Reg. Load Enable		1
Mem. Reg. Reset		1
Data Reg. Shift Clk.	1	1
Data Reg. Read Enable	1	1
Data Reg. Load Enable	1	1
Data Reg. & Output Reg. Reset	1	1
Output Reg. Shift Clk.	1	1
Output Reg. Load Enable	1	1
Temp. Store Increment	1	1
Temp. Store Shift Clk.	1	1
Temp. Store Read Enable	1	1
Temp. Store Load Enable	1	1
Temp. Store & Compare Reset	1	1

SEQUENCE GENERATOR ADDRESS	Inst. Reg	
	010	011
Compare Reg. Shift Clk.		
Compare Reg. Read Enable		
Compare Reg. Load Enable		
Read Memory		
Enable Scratch Pad	1	1
Write Scratch Pad	1	1
G/V → V		
Enable Comparator		
Reset Sequence Gen.		
Temp. Store Power	1	1
Comparator Power	1	1
Data Reg. Power	1	1
Count Command		
Reset Counter		
Stop		

SEQUENCE GENERATOR ADDRESS

Inst. Reg

011

01100

01101

01110

01111

10000

10001

10010

10011

10100

Compare Reg. Shift Clk.

Compare Reg. Read Enable

Compare Reg. Load Enable

Read Memory

Enable Scratch Pad

Write Scratch Pad

$G/V \rightarrow V$

Enable Comparator

Reset Sequence Gen.

Temp. Store Power

Comparator Power

Data Reg. Power

Count Command

Reset Counter

Stop

SEQUENCE GENERATOR ADDRESS	Inst. Reg	
	110	
Compare Reg. Shift Clk.	00101	
Compare Reg. Read Enable	00110	
Compare Reg. Load Enable	00111	
Read Memory	01000	
Enable Scratch Pad	01001	
Write Scratch Pad		
$G/V \rightarrow V$		
Enable Comparator		
Reset Sequence Gen.		
Temp. Store Power		
Comparator Power		
Data Reg. Power		
Count Command		
Reset Counter		
Stop		

Inst. Reg

110

00101

00110

0011

01000

01001

Compare Reg. Shift Clk.

Compare Reg. Read Enable

Compare Reg. Load Enable

Read Memory

Enable Scratch Pad

Write Scratch Pad

$$G/N \rightarrow V$$

Enable Comparator

Reset Sequence Gen.

Temp. Store Power

Comparator Power

Data Reg. Power

Count Command

Reset Counter

Stop

1

SEQUENCE GENERATOR
ADDRESS

Inst. Reg

110

00101

00110

00111

01000

01001

Instruction Ctr. Increment

Instr. Ctr. Shift Clk. Enable

Instr. Ctr. Read Enable

Instr. Ctr. Load Enable

Instr. Ctr. Reset

Memory Reg. Shift Clk.

Mem. Reg. Read Enable

Mem. Reg. Load Enable

Mem. Reg. Reset

Data Reg. Shift Clk.

Data Reg. Read Enable

Data Reg. Load Enable

Data Reg. & Output Reg. Reset

Output Reg. Shift Clk.

Output Reg. Load Enable

Temp. Store Increment

Temp. Store Shift Clk.

Temp. Store Read Enable

Temp. Store Load Enable

Temp. Store & Compare Reset

APPENDIX 4.3

TRIP REPORT – LSI VENDOR SURVEY

TRIP REPORT - LSI VENDOR SURVEY

The following Radiation personnel visited three MOS-LSI manufacturer's facilities on 12, 13, and 14 November 1969, for the purpose of obtaining design information relative to particular MAMS applications, evaluation of each vendors capability to supply reliable devices, and to obtain failure rate data.

Radiation Personnel

M. J. Slavin - Project Engineer
K. E. Farson - Design
G. E. Giles - Components Applications
D. B. McClain - Reliability

Each of the three vendors use essentially the same bonding processes consisting of die-to-package eutectic bonding and aluminum-to-aluminum ultrasonic wire bonds. Large quantity orders by commercial users, such as desktop computer manufacturers, are of primary interest to these vendors at the present time

American Micro-Systems, Inc. (AMI)

D. W. Yoder - Marketing Manager
J. Mingione - Product Marketing
J. Farley - Product Assurance Director

AMI has been in business three (3) years supplying strictly custom LSI devices. Their present facility has a pilot line capability of 30,000 to 40,000 devices per month. A new building is nearing completion with a production line capability of up to 10^6 devices per month. Wafers are obtained mainly from Texas Instrument.

AMI has good clean facilities and they claim to have the best equipment available for manufacturing and testing custom circuits. Jay Farley has previous experience in the semiconductor industry and is cognizant of the reliability problems associated with manufacturing MOS-LSI devices. He has a laboratory in which failure analysis can be performed. Jay estimates the failure rate of MOS arrays will vary between 0.01% per thousand hours and 0.1% per thousand hours depending on complexity and size. His estimate of failure mode distribution is 40% contamination, 30% metallization defects, and 30% miscellaneous such as test errors, etc. Efforts have been made by AMI to reduce contamination defects by passivating the chip. Metallization defects, intermittent or total opens caused by fracturing or migration are the more common symptoms, have been reduced by an improved method of controlling the thickness of metal-over-oxide steps. This method required that the metal be deposited at more than one angle.

The largest quantity user of AMI commercial custom circuits is the Burroughs Corporation in Plymouth, Michigan. A paper was presented at the August WESCON on the reliability of LSI by Ralph Parris of Burroughs.

The AIMP satellite program has provided the most pertinent data on system reliability. This Appendix contains data pertaining to NASA's experience in the program up to February 1969. AMI claims that these satellites have remained in orbit with no further failures, indicating a failure rate less than half that which is reported.

Fairchild Semiconductor

Howard Sharek - Customer Relations

Dick Kars - National Sales Rep.

Nick Phillon - Product Marketing

Rob Walker - Systems Design

Fairchild's new plant for LSI devices has been in operation for 1.5 years. The building has an area of 300,000 square feet, however, our tour included only the mask design area. Reliability personnel were not introduced during this visit, but Andy Procasini is Group Director of Rel/QC, Gil Bowers is Director of Discrete Circuits, and Charley Grey is Director of Integrated Circuits. Large quantity users of the Fairchild MOS LSI circuits are the Navy and Litton Industries. Fairchild is equipped for testing to MIL-STD-883 requirements. Appendix 4.5 is a test summary furnished by Fairchild that indicates an average failure rate of 0.2 percent per thousand hours if only the three catastrophic failures are considered and 0.5 percent per thousand hours considering all six failures. The metallization problem experienced on the VIP program with the Fairchild 9040 series devices has been reduced, and possibly eliminated, by an improved method of sloping the oxide steps to give a more uniform thickness of the metallization. Contamination problems are reduced by passivating the entire bottom of the package.

Electronic Arrays, Inc. (EA)

Dick Eiler - Product Applications

EA has been in operation 1.5 years manufacturing strictly standard off-the-shelf LSI circuits. They employ 125 people in a 27,000 square feet manufacturing area. Although not introduced, Sid Wiesner is the Rel/QA Manager who was formerly with Raytheon.

Large quantity users of the EA standard LSI circuits are NAFI (Submarines), Raytheon-Rhode Island (Military), G.E. - Syracuse (Military), and Hughes Aircraft. EA does not have facilities for testing to MIL-STD-883, however, these tests can be performed by an independent test facility. A 100 percent burn-in operation is performed at 150°C under voltage for a period of from eight to fourteen hours. EA claims there is no problem with increasing the burn-in time to 168 hours. They are equipped to perform failure analysis. Pre-cap visual is performed 100 percent. No test data was obtained during this visit, however, EA is preparing a reliability report that will present results of test data to date. This report is scheduled for release in January and Radiation will get a copy.

Summary and Conclusion

All three vendors have the organization and facility to build reliable LSI devices. AMI was the only vendor to introduce the product assurance representative, however, EA was very cooperative and our time schedule did not permit much more than a brief discussion and plant tour with the product applications representative. Fairchild was cooperative and offered organizational structure but no attempt was made to introduce the Rel/QA representative. All are equipped to analyze failures which is important since the Radiation Components Lab is not presently equipped to perform failure analysis of LSI devices.

APPENDIX 4.4

NASA/GSFC EXPERIENCE WITH AIMP MOSFETS

"MOSFET RELIABILITY - IMP SPACECRAFT"

by
Hosea D. White, Jr.
GSFC/NASA

In 1964 it was decided to build the AIMP D&E and IMP F&G encoding systems out of P channel MOSFETs. Since that time, over 26,000 cans have been purchased and three satellites have been placed in orbit. As of January 1, 1968 all three of the satellites are still in operation and have amassed 120 million MOSFET device hours. Two of the satellites have had no failures in the encoding system, while one of them (AIMP D) experienced two binary failures (one after 384 and the other after 458 days in orbit). It cannot be determined whether these failures were due to MOSFET failures or due to a mechanical short in the welded matrix. Thus it can be said that no failures occurred for 106 million hours and possibly have never occurred.

Since there are 2915 cans with 17,790 MOSFET devices still operating in orbit, the orbital device hours are building up at a rapid rate.

Two rather simple figurations were used in 8 pin TO-5 low profile cans as follows. A logic block with 3 devices per can, and a binary block with 12 devices per can. The encoders in AIMP D&E were identical with 257 binary cans and 489 logic cans for a total of 746 cans with 4551 devices for each payload. The encoder for IMP F had 491 binary cans and 932 logic cans for a total of 1423 cans with 8688 devices.

The results may be summarized as follows:

MOSFETS IN ORBIT (JANUARY 1, 1968)

<u>Payload</u>	<u>Cans</u>	<u>Devices/ Payload</u>	<u>Days in Orbit</u>	<u>Millions of Dev-Hours in Orbit</u>
AIMP D*	746	4551*	511*	56*
IMP F	1423	8688	221	46
AIMP E	746	4551	165	18
Total	2915	17790	897	120

* Possible binary failures after 384 and 458 days.

M E M O R A N D U M

4 January 1968

TO: Mr. Paul G. Marcotte
Project Manager AIMPFROM: Mr. Donald C. Lokerson
Code 711

SUBJ: ANALYSIS OF AIMP-D TELEMETRY FAILURES

A review of past failures after initial system assembly are shown in the table below.

<u>FAILURE NUMBER</u>	<u>CARD NUMBER</u>	<u>TIME OF FAILURE AFTER ASSEMBLY</u>	<u>LOCATION IN CARD</u>	<u>PROBABLE CAUSE</u>
1	01	1 week	Bit 5 U.I. Acc 1b,2b	*Mosfet
2	01	1 month	Analog Osc	*Zener Diode Failure
3	02	Assembly Checkout	U.I. Syne Pulse	*Short through Mylar
4	02	1 yr 9m & 1 yr 19d of flight	Bit 10 U.I. Acc 3b, 4b	Mosfet or Shorted Wires
5	02	2 yr & 1 yr 3m of flight	Bit 22 U.I. Acc 1b, 2b	Mosfet or Shorted Wires
6	03	2 Months	Acc 5a	*Short through Mylar
7	03	7 Months	Parity Check	Mosfet
8	04	2 Months	L258 U.I. Acc	*Mosfet

* - Known Cause of Failure

Thus of eight failures, 2 are known Mosfet failures and two are known shorted wires. Thus, the three failures not yet trouble-shot could be expected to be caused by one of those two causes.

Failures #1, 2 and 8 continued in the devices after removal from the circuit. Failures #3 and 6 continued until the suspected shorted wires were pried apart.

SUBJECT: ANALYSIS OF AIMP-D TELEMETRY FAILURES

Failure #4 occurred during flight with no known spacecraft perturbations at the time of failure. Figure 1 is a copy of the module matrix expanded 4 times larger than actual size. A search for a failure due to shorting wires reveals only one possibility of great likelihood. The pin 4 of B230 (same as B130 in layout) could short to pin 3 by a puncture or "cold flow" of the mylar from the potting pressure as shown in figure 2. This would prevent the binary from staying in the "one" state or from binating after reset was removed. Since Failures 3 and 6 were of this same type, at least 50% probability of this being the cause of failure might be surmised. It is also possible a failure in the chip is equally likely.

Failure #5 occurred during flight with no known spacecraft perturbations at the time of failure. Figure 1 shows the region of this failure also. A search for a failure due to shorting wires reveals only one possibility of great likelihood. The pin 1 of B163 could short to pin 8 if the wire was not cut off accurately and within .03 inches of the weld. Our welding inspector feels this is a good possibility. Possibly the potting pressure deformed the resistor load to help cause the problem. No other short seems likely which would cause the binary to stay in the "one" state. This failure would cause the previous binary to stay in the "zero" state - a condition which appears to be met by all data I have examined to date. It is also possible a failure in the chip is equally likely.

Failure #7 occurred in the flyable back-up AIMP-E during system integration, and is not accessible for trouble-shooting. The failure is in B22, such that it is held in the "1" state, but the previous flip-flop operates properly. Thus, no short appears likely to cause these conditions from looking at the matrix in figure 4. Thus, the most likely failure appears to be within the Mosfet chip. An open wire or resistor to pin 3 of B22 is an unlikely possibility, which would produce this condition.

This analysis plus the failure analysis experience on the AIMP encoders demonstrates the need to avoid particular mechanical layouts in future designs and has shown that after final assembly and potting, the main mode of Mosfet failure has been corrosion of the chip due to poor chemical wash-off procedures, (failure analysis reports 556, 325) as shown in figures 5 and 6.

The over-all flight reliability is remarkably good, with two failures (neither of which are proved to be Mosfet failures), and 106 million Mosfet device hours in flight as of January 1, 1968. Flyable hardware built to date includes about 48,819 Mosfet devices.

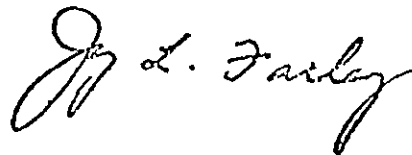
/s/ Donald C. Lokerson

Enclosures

cc: Dr. Ness	Dr. Van Allen (U/I)	Mr. Camp (U/I)
Mr. Butler	Mr. Ripley	R. Broadhurst (Bird)
Mr. Madden	Mr. Brahm	J. Gouge, Jr. (Bird)
Dr. Rochelle	Mr. Van Allen	H. White
J. Lyons	F. Kreis	

ADDENDUM

Regarding NASA's experience using some of the earlier and less reliable MOS parts, I think their success has been due to the fact that the circuit designers and systems people believed in MOS. I am updating the failure rate that Hosea White quotes in his report. During the period covered by Mr. White's report, 2915 MOS cans had survived 897 days in orbit for a can failure rate of .005% per thousand hours at the 60% confidence level. This failure rate is derived from an assumed two failures out of $.63 \times 10^6$ can hours. The two failures did occur, but NASA is not sure whether or not they were semiconductor failures or harnessing failures. The two failures occurred after one year in orbit. Since that time, the same 2915 devices have accumulated at least another 390 days in orbit. This brings the can hours up to 92×10^6 . The operational failure rate with no additional failures becomes .0035% per thousand hours. The actual failure rate per transistor is .001%. If indeed these failures were not due to MOS parts, the failure rate observed goes down to .0003% per thousand hours. It should be kept in mind that these parts were made with thin oxide technology and without the know-how we have today. It is easy to presume a reliability improvement of one order of magnitude.



Jay L. Farley
Director of Product Assurance

February 27, 1969

APPENDIX 4.5

TEST SUMMARY OF FAIRCHILD STANDARD LSI CIRCUITS

*

Product Code	Device Function	No. of Devices	Operating Life Test Conditions	Test Hours	Device Hours	Current Status	Failures Observed
3102	3-input Nand gate	55	$T_A = +85^\circ\text{C}$, $V_{DD} = -30\text{V}$, ring counter & flip-flops	12,440	684,200	Continuing	0
3304	Dual 16-bit static Shift Register	28	$T_A = +85^\circ\text{C}$, $V_{DD} = 13\text{V}$, $V_{GG} = -27\text{V}$ $V_{\text{clock}} = -27\text{V}$, ring counter	6,320	176,960	Continuing	1*
3320	64-bit dynamic Shift Register	40	$T_A = +85^\circ\text{C}$, $V_{\text{clock}} = +27\text{V}$ ring counter	6,320	252,800	Continuing	1*
3501	1024-bit read-only-memory	20	$T_A = +85^\circ\text{C}$, $V_{DD} = -13\text{V}$, $V_{GG} = -27\text{V}$ $V = -27\text{V}$ operating in a 128-word by 8-bit format	980	19,600	Continuing	0
3700	4 Channel Multiplexer	55	$T_A = +125^\circ\text{C}$, $V_{DD} = 30\text{V}$, $V_D = 10\text{V}$ ring counter	12,600	693,000	Continuing	0
3701	6 Channel Multiplexer	51	$T_A = +125^\circ\text{C}$, $V_D = +30\text{V}$ High temp back bias	2,875	146,625	Terminated	3**
3708	8 Channel Multiplexer (Silicon-gate process)	14	$T_A = +85^\circ\text{C}$, $V_{DD} = -25\text{V}$ $V_{SS} = 0\text{V}$ 8-channel Switching operation	2,500	35,000	Continuing	0
3750	10-bit D/A Converter	19	$T_A = +85^\circ\text{C}$, $V_{GG} = -27\text{V}$, $V_{\text{clock}} = -27\text{V}$, ring counter	7,016	133,304	Continuing	2***
Total	All types	282		51,051	2,141,489		3*

Failure rate all types at 60% confidence level 0.19%/1000 hours

* Catastrophic failures

** Failing to meet spec limits of gate leakage current - functionally good.

*** One catastrophic failure, one destroyed during data acquisition.